

# 74LV125

Quad buffer/line driver; 3-state

Rev. 03 — 7 April 2009

Product data sheet

## 1. General description

The 74LV125 is a low-voltage Si-gate CMOS device that is pin and function compatible with 74HC125 and 74HCT125.

The 74LV125 provides four non-inverting buffer/line drivers with 3-state outputs. The 3-state outputs ( $nY$ ) are controlled by the output enable input ( $n\overline{OE}$ ). A HIGH at  $n\overline{OE}$  causes the outputs to assume a high-impedance OFF-state.

## 2. Features

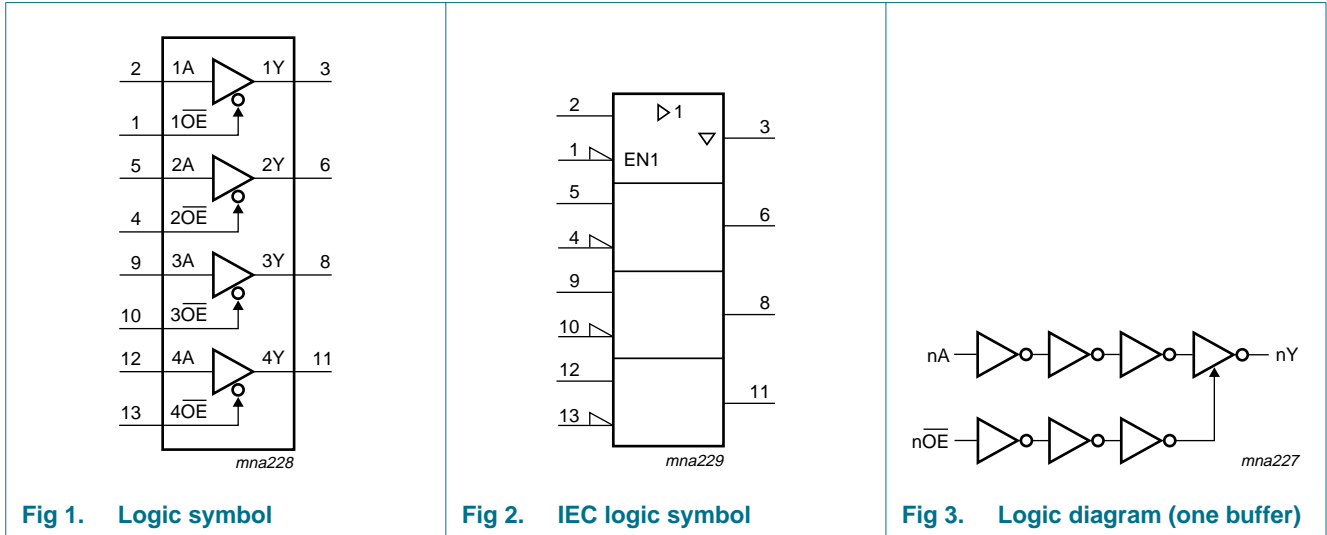
- Wide operating voltage: 1.0 V to 5.5 V
- Optimized for low voltage applications: 1.0 V to 3.6 V
- Accepts TTL input levels between  $V_{CC} = 2.7$  V and  $V_{CC} = 3.6$  V
- Typical output ground bounce < 0.8 V at  $V_{CC} = 3.3$  V and  $T_{amb} = 25$  °C
- Typical HIGH-level output voltage ( $V_{OH}$ ) undershoot: > 2 V at  $V_{CC} = 3.3$  V and  $T_{amb} = 25$  °C
- ESD protection:
  - ◆ HBM JESD22-A114E exceeds 2000 V
  - ◆ MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from  $-40$  °C to  $+85$  °C and from  $-40$  °C to  $+125$  °C

## 3. Ordering information

Table 1. Ordering information

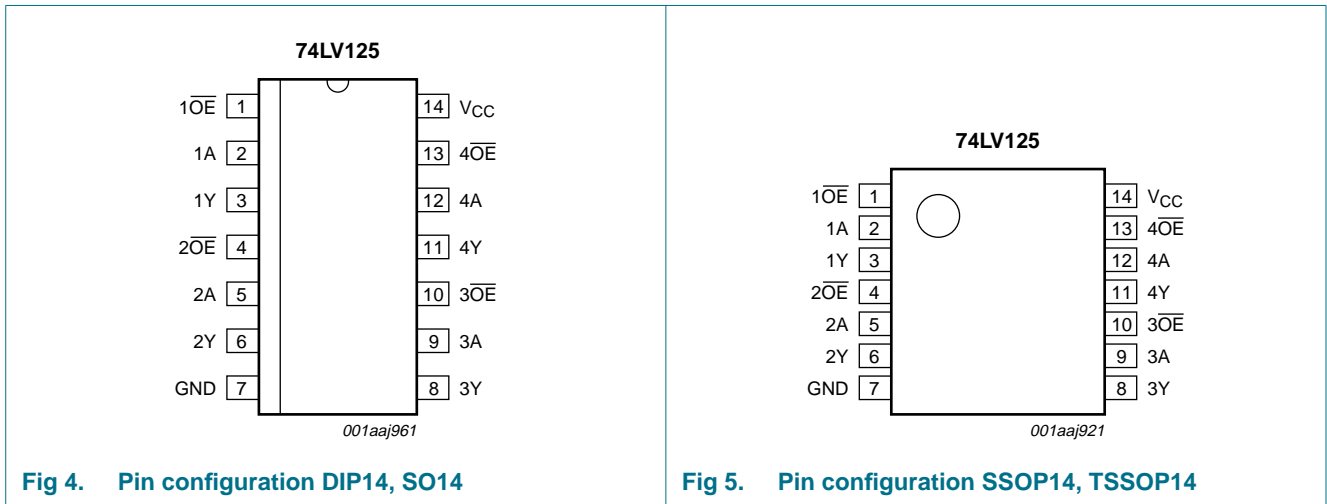
Type number	Package			
	Temperature range	Name	Description	Version
74LV125N	$-40$ °C to $+125$ °C	DIP14	plastic dual in-line package; 14 leads (300 mil)	SOT27-1
74LV125D	$-40$ °C to $+125$ °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74LV125DB	$-40$ °C to $+125$ °C	SSOP14	plastic shrink small outline package; 14 leads; body width 5.3 mm	SOT337-1
74LV125PW	$-40$ °C to $+125$ °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1

4. Functional diagram



5. Pinning information

5.1 Pinning



## 5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
$1\overline{OE}$ , $2\overline{OE}$ , $3\overline{OE}$ , $4\overline{OE}$ ,	1, 4, 10, 13	output enable input (active LOW)
1A, 2A, 3A, 4A	2, 5, 9, 12	data input
1Y, 2Y, 3Y, 4Y	3, 6, 8, 11	data output
GND	7	ground (0 V)
$V_{CC}$	14	supply voltage

## 6. Functional description

Table 3. Function table<sup>[1]</sup>

Control	Input	Output
$n\overline{OE}$	nA	nY
L	L	L
L	H	H
H	X	Z

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

## 7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+7.0	V
$I_{IK}$	input clamping current	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$	[1] -	±20	mA
$I_{OK}$	output clamping current	$V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$	[1] -	±50	mA
$I_O$	output current	$V_O = -0.5\text{ V}$ to $(V_{CC} + 0.5\text{ V})$	-	±35	mA
$I_{CC}$	supply current		-	70	mA
$I_{GND}$	ground current		-70	-	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40\text{ °C}$ to $+125\text{ °C}$	[2]		
		DIP14	-	750	mW
		SO14, SSOP14, TSSOP14	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For DIP14 packages: above 70 °C the value of  $P_{tot}$  derates linearly with 12 mW/K.  
 For SO14 packages: above 70 °C the value of  $P_{tot}$  derates linearly with 8 mW/K.  
 For (T)SSOP14 packages: above 60 °C the value of  $P_{tot}$  derates linearly with 5.5 mW/K.

## 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC}$	supply voltage <sup>[1]</sup>		1.0	3.3	5.5	V
$V_I$	input voltage		0	-	$V_{CC}$	V
$V_O$	output voltage		0	-	$V_{CC}$	V
$T_{amb}$	ambient temperature		-40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 1.0\text{ V to }2.0\text{ V}$	-	-	500	ns/V
		$V_{CC} = 2.0\text{ V to }2.7\text{ V}$	-	-	200	ns/V
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	-	-	100	ns/V
		$V_{CC} = 3.6\text{ V to }5.5\text{ V}$	-	-	50	ns/V

[1] The static characteristics are guaranteed from  $V_{CC} = 1.2\text{ V}$  to  $V_{CC} = 5.5\text{ V}$ , but LV devices are guaranteed to function down to  $V_{CC} = 1.0\text{ V}$  (with input levels GND or  $V_{CC}$ ).

## 9. Static characteristics

**Table 6. Static characteristics**

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Max	
$V_{IH}$	HIGH-level input voltage	$V_{CC} = 1.2\text{ V}$	0.9	-	-	0.9	-	V
		$V_{CC} = 2.0\text{ V}$	1.4	-	-	1.4	-	V
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	2.0	-	-	2.0	-	V
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	$0.7V_{CC}$	-	-	$0.7V_{CC}$	-	V
$V_{IL}$	LOW-level input voltage	$V_{CC} = 1.2\text{ V}$	-	-	0.3	-	0.3	V
		$V_{CC} = 2.0\text{ V}$	-	-	0.6	-	0.6	V
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	-	-	0.8	-	0.8	V
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	-	-	$0.3V_{CC}$	-	$0.3V_{CC}$	V
$V_{OH}$	HIGH-level output voltage	$V_I = V_{IH}$ or $V_{IL}$						
		$I_O = -100\ \mu\text{A}; V_{CC} = 1.2\text{ V}$	-	1.2	-	-	-	V
		$I_O = -100\ \mu\text{A}; V_{CC} = 2.0\text{ V}$	1.8	2.0	-	1.8	-	V
		$I_O = -100\ \mu\text{A}; V_{CC} = 2.7\text{ V}$	2.5	2.7	-	2.5	-	V
		$I_O = -100\ \mu\text{A}; V_{CC} = 3.0\text{ V}$	2.8	3.0	-	2.8	-	V
		$I_O = -100\ \mu\text{A}; V_{CC} = 4.5\text{ V}$	4.3	4.5	-	4.3	-	V
		$I_O = -8\text{ mA}; V_{CC} = 3.0\text{ V}$	2.4	2.82	-	2.2	-	V
$I_O = -16\text{ mA}; V_{CC} = 4.5\text{ V}$	3.6	4.2	-	3.5	-	V		

**Table 6. Static characteristics ...continued**

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Max	
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>						
		I <sub>O</sub> = 100 μA; V <sub>CC</sub> = 1.2 V	-	0	-	-	-	V
		I <sub>O</sub> = 100 μA; V <sub>CC</sub> = 2.0 V	-	0	0.2	-	0.2	V
		I <sub>O</sub> = 100 μA; V <sub>CC</sub> = 2.7 V	-	0	0.2	-	0.2	V
		I <sub>O</sub> = 100 μA; V <sub>CC</sub> = 3.0 V	-	0	0.2	-	0.2	V
		I <sub>O</sub> = 100 μA; V <sub>CC</sub> = 4.5 V	-	0	0.2	-	0.2	V
		I <sub>O</sub> = 8 mA; V <sub>CC</sub> = 3.0 V	-	0.20	0.40	-	0.50	V
		I <sub>O</sub> = 16 mA; V <sub>CC</sub> = 4.5 V	-	0.35	0.55	-	0.65	V
I <sub>I</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 5.5 V	-	-	1.0	-	1.0	μA
I <sub>OZ</sub>	OFF-state output current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 5.5 V	-	-	5	-	10	μA
I <sub>CC</sub>	supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 5.5 V	-	-	20	-	160	μA
ΔI <sub>CC</sub>	additional supply current	per input; V <sub>I</sub> = V <sub>CC</sub> - 0.6 V; V <sub>CC</sub> = 2.7 V to 3.6 V	-	-	500	-	850	μA
C <sub>I</sub>	input capacitance		-	3.5	-	-	-	pF

[1] Typical values are measured at T<sub>amb</sub> = 25 °C.

## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**

Voltages are referenced to GND (ground = 0 V). For test circuit see [Figure 8](#).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Max	
t <sub>pd</sub>	propagation delay	nA to nY; see <a href="#">Figure 6</a> <sup>[2]</sup>						
		V <sub>CC</sub> = 1.2 V	-	55	-	-	-	ns
		V <sub>CC</sub> = 2.0 V	-	19	24	-	31	ns
		V <sub>CC</sub> = 2.7 V	-	14	18	-	23	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V; C <sub>L</sub> = 15 pF <sup>[3]</sup>	-	9	-	-	-	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V <sup>[3]</sup>	-	10	14	-	18	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V	-	-	12	-	15	ns
t <sub>en</sub>	enable time	nOE to nY; see <a href="#">Figure 7</a> <sup>[2]</sup>						
		V <sub>CC</sub> = 1.2 V	-	75	-	-	-	ns
		V <sub>CC</sub> = 2.0 V	-	26	31	-	39	ns
		V <sub>CC</sub> = 2.7 V	-	19	23	-	29	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V <sup>[3]</sup>	-	14	18	-	23	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V	-	-	15	-	19	ns

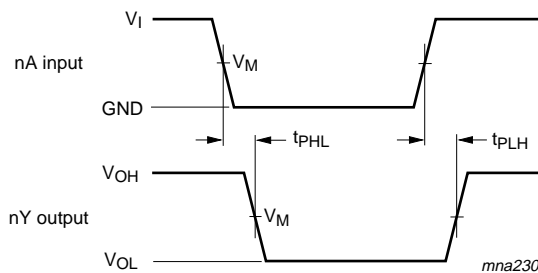
**Table 7. Dynamic characteristics ...continued**

Voltages are referenced to GND (ground = 0 V). For test circuit see [Figure 8](#).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Max	
t <sub>dis</sub>	disable time	nOE to nY; see <a href="#">Figure 7</a> <sup>[2]</sup>						
		V <sub>CC</sub> = 1.2 V	-	65	-	-	-	ns
		V <sub>CC</sub> = 2.0 V	-	24	32	-	39	ns
		V <sub>CC</sub> = 2.7 V	-	18	24	-	29	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V <sup>[3]</sup>	-	14	20	-	24	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V	-	-	17	-	21	ns
C <sub>PD</sub>	power dissipation capacitance	C <sub>L</sub> = 50 pF; f <sub>i</sub> = 1 MHz; V <sub>I</sub> = GND to V <sub>CC</sub> ; V <sub>CC</sub> = 3.3 V <sup>[4]</sup>	-	22	-	-	-	pF

- [1] All typical values are measured at T<sub>amb</sub> = 25 °C.
- [2] t<sub>pd</sub> is the same as t<sub>PLH</sub> and t<sub>PHL</sub>.  
t<sub>en</sub> is the same as t<sub>PZL</sub> and t<sub>PZH</sub>.  
t<sub>dis</sub> is the same as t<sub>PLZ</sub> and t<sub>PHZ</sub>.
- [3] Typical values are measured at nominal supply voltage (V<sub>CC</sub> = 3.3 V).
- [4] C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW).  
P<sub>D</sub> = C<sub>PD</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>i</sub> × N + Σ(C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) where:  
f<sub>i</sub> = input frequency in MHz, f<sub>o</sub> = output frequency in MHz  
C<sub>L</sub> = output load capacitance in pF  
V<sub>CC</sub> = supply voltage in Volts  
N = number of inputs switching  
Σ(C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of the outputs.

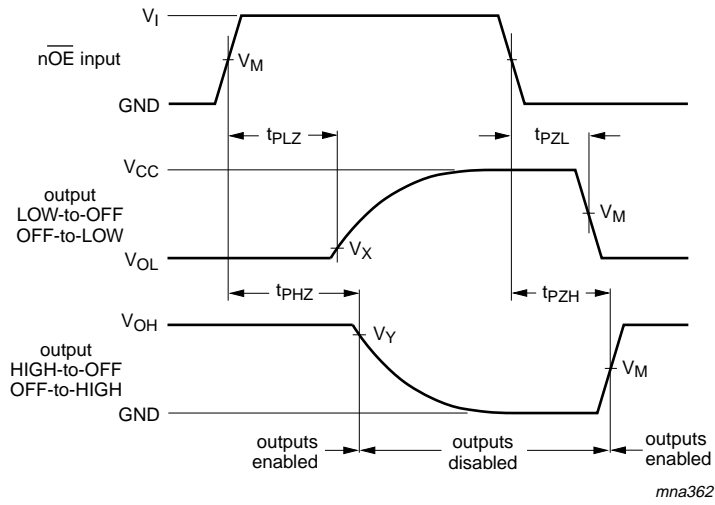
## 11. Waveforms



Measurement points are given in [Table 8](#).

V<sub>OL</sub> and V<sub>OH</sub> are typical voltage output levels that occur with the output load.

**Fig 6. The input (nA) to output (nY) propagation delays**



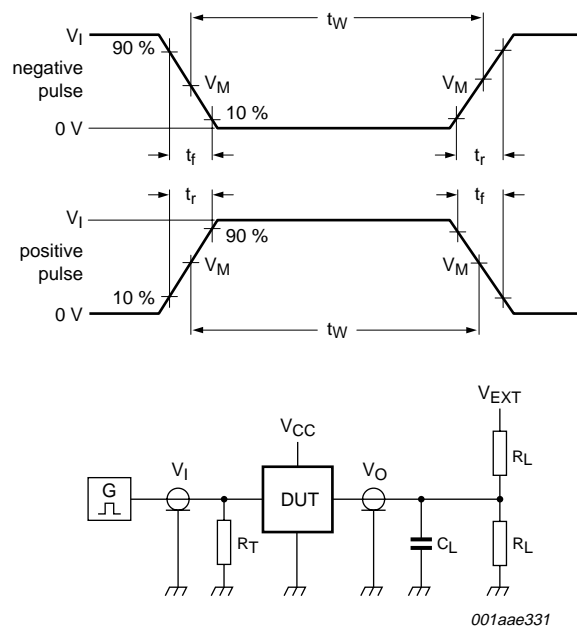
Measurement points are given in [Table 8](#).

$V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

**Fig 7. Enable and disable times**

**Table 8. Measurement points**

Supply voltage	Input	Output		
$V_{CC}$	$V_M$	$V_M$	$V_X$	$V_Y$
< 2.7 V	$0.5V_{CC}$	$0.5V_{CC}$	$V_{OL} + 0.1V_{CC}$	$V_{OH} - 0.1V_{CC}$
2.7 V to 3.6 V	1.5 V	1.5 V	$V_{OL} + 0.3 V$	$V_{OH} - 0.3 V$
$\geq 4.5 V$	$0.5V_{CC}$	$0.5V_{CC}$	$V_{OL} + 0.1V_{CC}$	$V_{OH} - 0.1V_{CC}$



Test data is given in [Table 9](#).

Definitions for test circuit:

$R_L$  = Load resistance.

$C_L$  = Load capacitance including jig and probe capacitance.

$R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

$V_{EXT}$  = External voltage for measuring switching times.

**Fig 8. Load circuit for measuring switching times**

**Table 9. Test data**

Supply voltage	Input		Load		$V_{EXT}$		
$V_{CC}$	$V_I$	$t_r, t_f$	$C_L$	$R_L$	$t_{PHL}, t_{PLH}$	$t_{PZH}, t_{PHZ}$	$t_{PZL}, t_{PLZ}$
< 2.7 V	$V_{CC}$	$\leq 2.5$ ns	50 pF	1 k $\Omega$	open	GND	$2V_{CC}$
2.7 V to 3.6 V	2.7 V	$\leq 2.5$ ns	15 pF, 50 pF	1 k $\Omega$	open	GND	$2V_{CC}$
$\geq 4.5$ V	$V_{CC}$	$\leq 2.5$ ns	50 pF	1 k $\Omega$	open	GND	$2V_{CC}$



12. Package outline

DIP14: plastic dual in-line package; 14 leads (300 mil)

SOT27-1

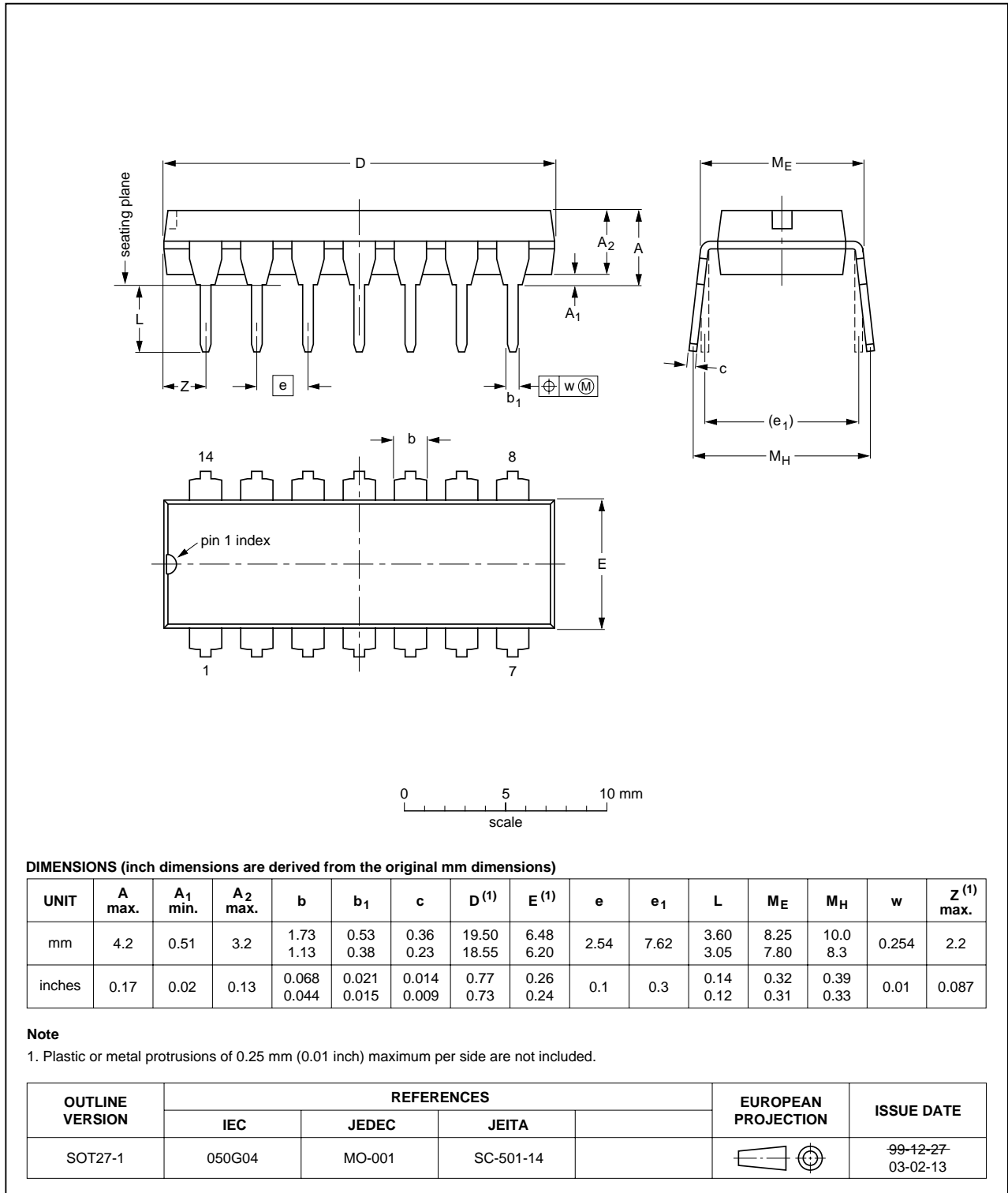


Fig 9. Package outline SOT27-1 (DIP14)

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

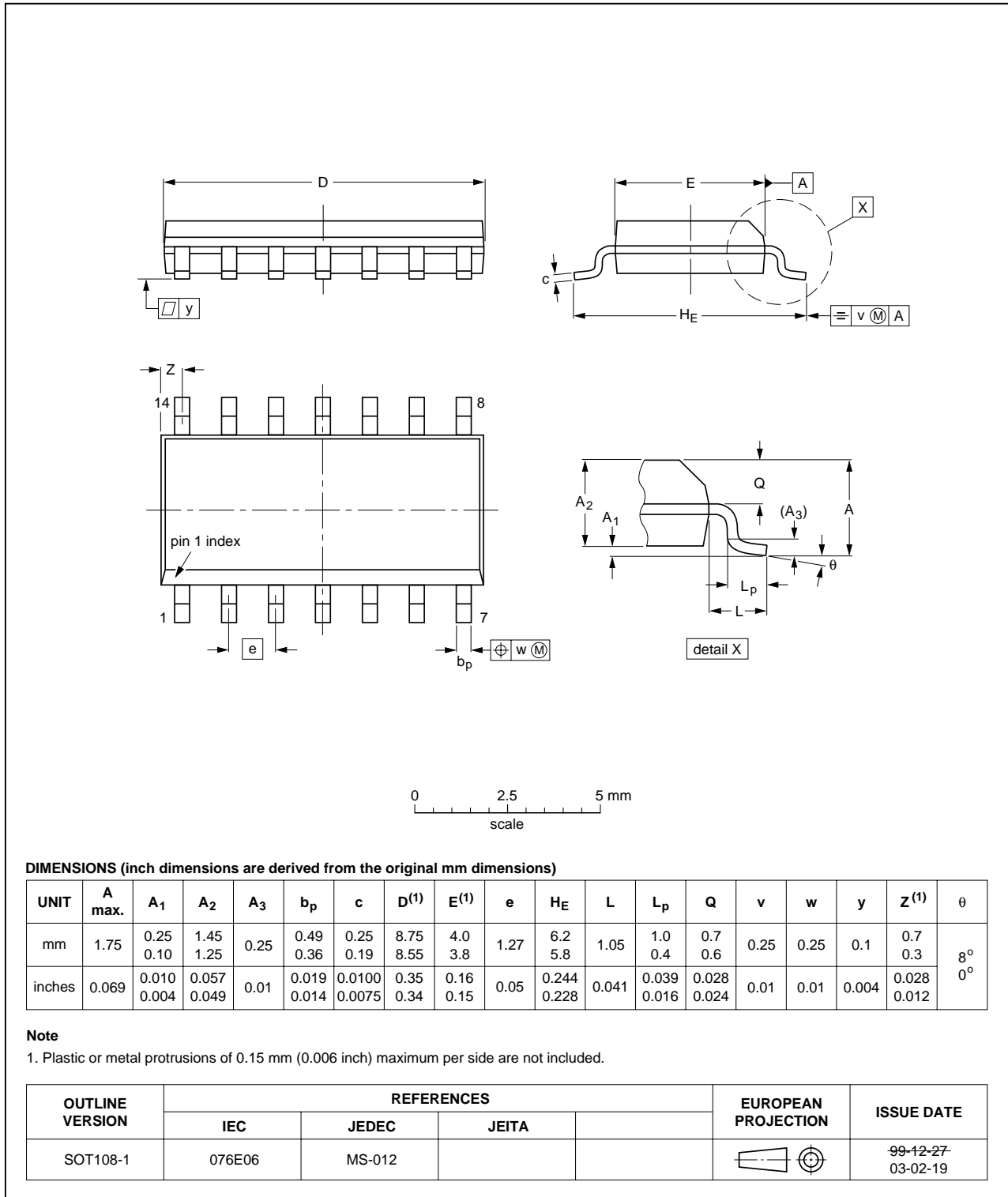


Fig 10. Package outline SOT108-1 (SO14)

SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm

SOT337-1

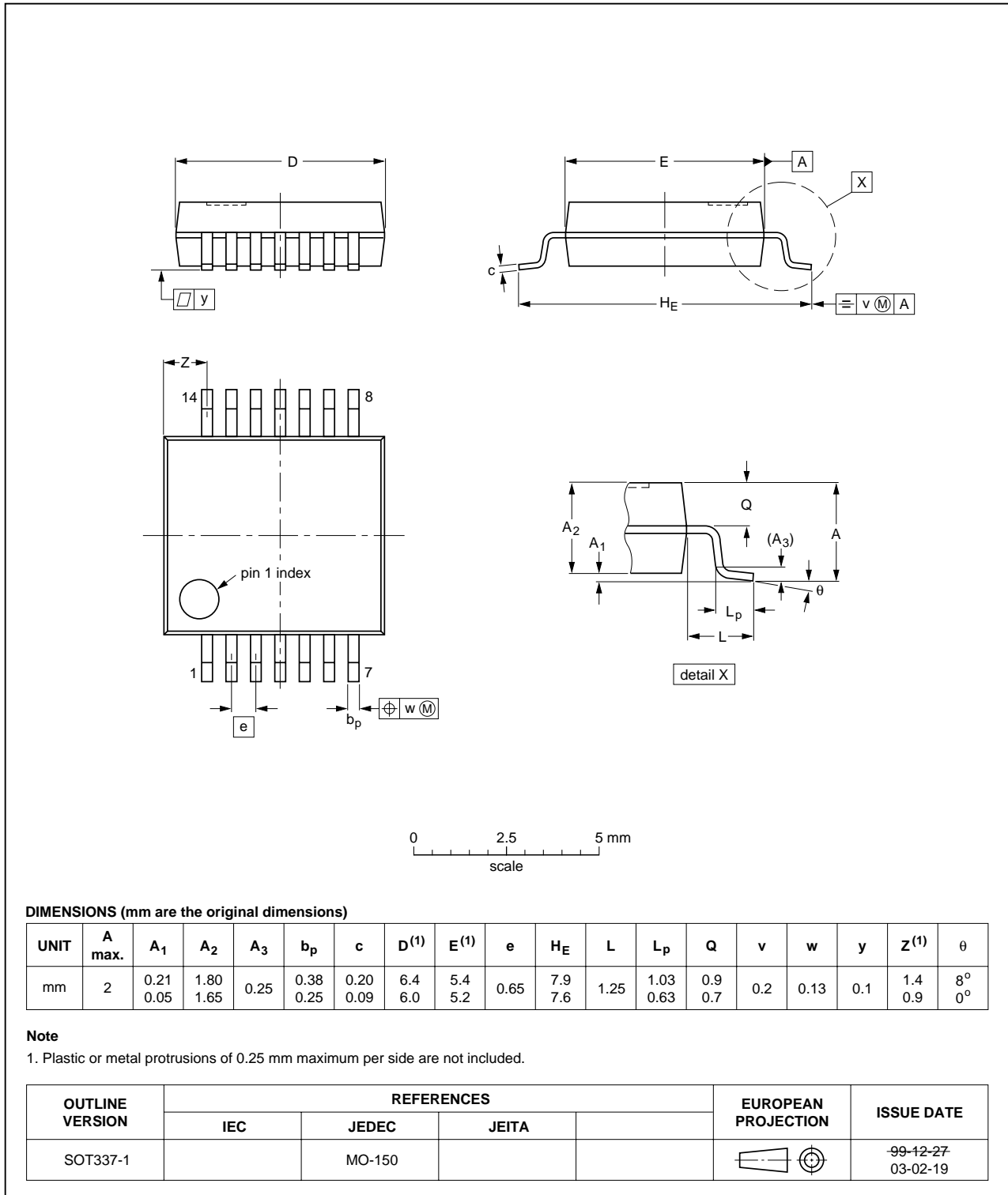


Fig 11. Package outline SOT337-1 (SSOP14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

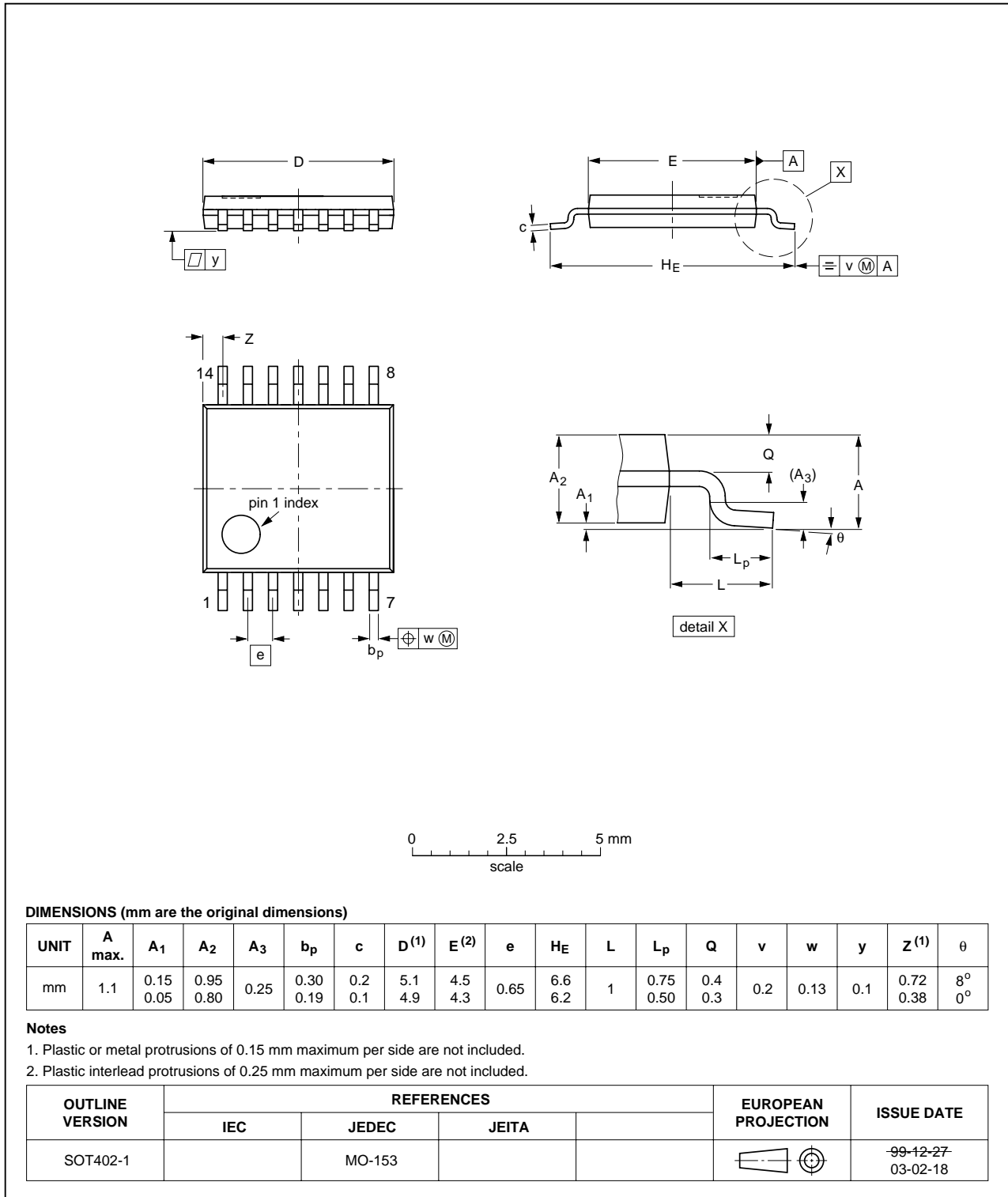


Fig 12. Package outline SOT402-1 (TSSOP14)

## 13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

## 14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LV125_3	20090407	Product data sheet	-	74LV125_2
Modifications:	<ul style="list-style-type: none"><li>The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li><li>Legal texts have been adapted to the new company name when appropriate.</li></ul>			
74LV125_2	19980428	Product specification	-	74LV125_1
74LV125_1	19970203	Product specification	-	-

## 15. Legal information

### 15.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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