PRECISION N-CHANNEL EPAD® MOSFET ARRAY

QUAD HIGH DRIVE MATCHED PAIR

$V_{GS(th)}$= +0.80V

GENERAL DESCRIPTION

The ALD210808A/ALD210808 precision enhancement mode N-Channel EPAD® MOSFET array is precision matched at the factory using ALD's proven EPAD® CMOS technology. These quad monolithic devices are enhanced additions to the ALD110808A/ALD110808 EPAD® MOSFET Family, with increased forward transconductance and output conductance, particularly at very low supply voltages.

Intended for low voltage, low power small signal applications, the ALD210808A/ALD210808 features precision threshold voltage, which enables circuit designs with input/output signals referenced to GND at enhanced operating voltage ranges. With these devices, a circuit with multiple cascading stages can be built to operate at extremely low supply/bias voltage levels. For example, a nanopower input amplifier stage operating at less than 1.0V supply voltage has been successfully built with these devices.

ALD210808A EPAD MOSFETs feature exceptional matched pair electrical characteristics of Gate Threshold Voltage $V_{GS(th)}$ set precisely at +0.80V ±0.01V, I_{DS} = +10μA @ V_{DS} = 0.1V, with a typical offset voltage of only ±0.001V (1mV). Built on a single monolithic chip, they also exhibit excellent temperature tracking characteristics. These precision devices are versatile as design components for a broad range of analog small signal applications such as basic building blocks for current mirrors, matching circuits, current sources, differential amplifier input stages, transmission gates, and multiplexers. They also excel in limited operating voltage applications, such as very low level voltage-clamps and nano-power normally-on circuits.

In addition to precision matched-pair electrical characteristics, each individual EPAD MOSFET also exhibits well controlled manufacturing characteristics, enabling the user to depend on tight design limits from different production batches. These devices are built for minimum offset voltage and differential thermal response, and they can be used for switching and amplifying applications in +0.1V to +10V (±0.05V to ±5V) powered systems where low input bias current, low input capacitance, and fast switching speed are desired. At V_{GS} > +0.80V, the device exhibits enhancement mode characteristics whereas at V_{GS} < +0.80V the device operates in the subthreshold voltage region and exhibits conventional sub threshold characteristics, with well controlled turn-off and sub-threshold levels that operate the same as standard enhancement mode MOSFETs.

The ALD210808A/ALD210808 features high input impedance ($2.5 \times 10^{10}\Omega$) and high DC current gain ($>10^8$). A sample calculation of the DC current gain at a drain output current of 30mA and input current of 300pA at 25°C is 30mA/300pA = 100,000,000, which translates into a dynamic operating current range of about eight orders of magnitude. A series of four graphs titled "Forward Transfer Characteristics", with the 2nd and 3rd sub-titled "expanded (subthreshold)" and "further expanded (subthreshold)", and the 4th sub-titled "low voltage", illustrates the wide dynamic operating range of these devices.

Generally it is recommended that the V+ pin be connected to the most positive voltage and the V- and IC (internally-connected) pins to the most negative voltage in the system. All other pins must have voltages within these voltage limits at all times. Standard ESD protection facilities and handling procedures for static sensitive devices are highly recommended when using these devices.

ORDERING INFORMATION ("L" suffix denotes lead-free (RoHS))

Operating Temperature Range * 0°C to +70°C	
16-Pin SOIC Package	16-Pin Plastic Dip Package
ALD210808ASCL ALD210808SCL	ALD210808APCL ALD210808PCL

*Contact factory for industrial temp. range or user-specified threshold voltage values.

FEATURES & BENEFITS

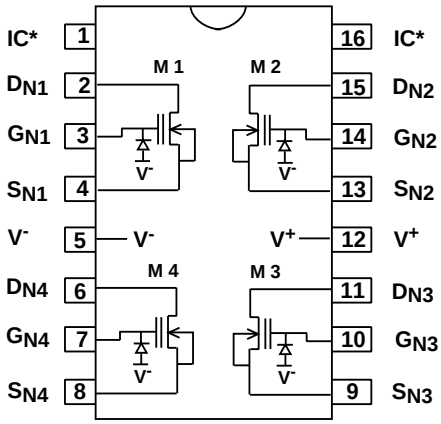
- Precision $V_{GS(th)}$ = +0.80V ±0.010V
- V_{OS} ($V_{GS(th)}$ match) to 2mV/10mV max.
- Sub-threshold voltage (nano-power) operation
- < 800mV min. operating voltage
- < 1nA min. operating current
- < 1nW min. operating power
- > 100,000,000:1 operating current ranges
- High transconductance and output conductance
- Low $R_{DS(ON)}$ of 25Ω
- Output current > 50mA
- Matched and tracked tempco
- Tight lot-to-lot parametric control
- Positive, zero, and negative $V_{GS(th)}$ tempco
- Low input capacitance and leakage currents

APPLICATIONS

- Low overhead current mirrors and current sources
- Zero Power Normally-On circuits
- Energy harvesting detectors
- Very low voltage analog and digital circuits
- Zero power fail-safe circuits
- Backup battery circuits & power failure detector
- Extremely low level voltage-clamps
- Extremely low level zero-crossing detectors
- Matched source followers and buffers
- Precision current mirrors and current sources
- Matched capacitive probes and sensor interfaces
- Charge detectors and charge integrators
- High gain differential amplifier input stage
- Matched peak-detectors and level-shifters
- Multiple Channel Sample-and-Hold switches
- Precision Current multipliers
- Discrete matched analog switches/multiplexers
- Nanopower discrete voltage comparators

PIN CONFIGURATION

ALD210808



SCL, PCL PACKAGES

*IC pins are internally connected, connect to V-

ABSOLUTE MAXIMUM RATINGS

Drain-Source voltage, V_{DS} ——— 10.6V
Gate-Source voltage, V_{GS} ——— 10.6V
Operating Current ——— 80mA
Power dissipation ——— 500mW
Operating temperature range SCL, PCL ——— 0°C to +70°C
Storage temperature range ——— -65°C to +150°C
Lead temperature, 10 seconds ——— +260°C

CAUTION: ESD Sensitive Device. Use static control procedures in ESD controlled environment.

OPERATING ELECTRICAL CHARACTERISTICS

V^+ = +5V V^- = GND T_A = 25°C unless otherwise specified

Parameter	Symbol	ALD210808A			ALD210808			Unit	Test Conditions
		Min	Typ	Max	Min	Typ	Max		
Gate Threshold Voltage	$V_{GS(th)}$	0.78	0.80	0.82	0.78	0.80	0.82	V	I_{DS} = 10μA, V_{DS} = 0.1V
Offset Voltage	V_{OS}		1	2		2	10	mV	$V_{GS(th)M1}$ - $V_{GS(th)M2}$ or $V_{GS(th)M3}$ - $V_{GS(th)M4}$
Offset Voltage Tempco	TC_{VOS}		5			5		μV/°C	V_{DS1} = V_{DS2}
Gate Threshold Voltage Tempco	$TC_{VGS(th)}$		-1.6 0.0 +1.6			-1.6 0.0 +1.6		mV/°C	I_D = 10μA, V_{DS} = 0.1V I_D = 380μA, V_{DS} = 0.1V I_D = 700μA, V_{DS} = 0.1V
Drain Source On Current	$I_{DS(ON)}$		70			70		mA	V_{GS} = +4.8V, V_{DS} = +5V
			50			50		μA	V_{GS} = +0.9V, V_{DS} = +0.1V
Forward Transconductance	G_{FS}		24			24		mmho	V_{GS} = +4.8V V_{DS} = +5.0V
Transconductance Mismatch	ΔG_{FS}		1.8			1.8		%	
Output Conductance	G_{OS}		1.6			1.6		mmho	V_{GS} = +4.8V V_{DS} = +5.0V
Drain Source On Resistance	$R_{DS(ON)}$		25			25		Ω	V_{GS} = +5.8V V_{DS} = +0.1V
Drain Source On Resistance	$R_{DS(ON)}$		10 2.0			10 2.0		KΩ	V_{GS} = +0.8V, V_{DS} = +0.1V V_{GS} = +0.9V, V_{DS} = +0.1V
Drain Source On Resistance Tolerance	$\Delta R_{DS(ON)}$		1.8			1.8		%	V_{GS} = +5.8V V_{DS} = +0.1V
Drain Source On Resistance Mismatch	$\Delta R_{DS(ON)}$		0.6			0.6		%	
Drain Source Breakdown Voltage	BV_{DSX}	10			10			V	V^- = V_{GS} = -0.2V I_{DS} = 10μA
Drain Source Leakage Current[1]	$I_{DS(OFF)}$		10	400 4		10	400 4	pA nA	V_{GS} = -0.2V, V_{DS} = +5V V^- = -5V T_A = 125°C
Gate Leakage Current[1]	I_{GSS}		5	200 1		5	200 1	pA nA	V_{GS} = +5V, V_{DS} = 0V T_A = 125°C
Input Capacitance	C_{ISS}		15			15		pF	
Transfer Reverse Capacitance	C_{RSS}		1			1		pF	
Turn-on Delay Time	t_{on}		10			10		ns	V^+ = 5V, R_L = 5KΩ
Turn-off Delay Time	t_{off}		10			10		ns	V^+ = 5V, R_L = 5KΩ
Crosstalk			60			60		dB	f = 100KHz

Notes: [1] Consists of junction leakage currents

PERFORMANCE CHARACTERISTICS OF EPAD®
PRECISION MATCHED PAIR MOSFET ARRAY FAMILY

ALD2108xx/ALD2129xx/ALD2148xx/ALD2169xx high precision monolithic quad/dual N-Channel MOSFET arrays are enhanced versions of the ALD1108xx/ALD1109xx EPAD® MOSFET family, with increased forward transconductance and output conductance, intended for operation at very low power supply voltages. These devices are also capable of sub-threshold operation with less than 1nA of operating supply currents and at the same time delivering higher output drive currents (typ. > 50mA). They feature precision Gate Offset Voltages, V_{OS} , defined as the difference in $V_{GS(th)}$ between MOSFET pairs M1 and M2 or M3 and M4.

ALD's Electrically Programmable Analog Device (EPAD®) technology provides the industry's only family of matched MOSFET transistors with a range of precision gate-threshold voltage values. All members of this family are designed and actively programmed for exceptional matching of device electrical and temperature characteristics. Gate Threshold Voltage $V_{GS(th)}$ values range from -3.50V Depletion Mode to +3.50V Enhancement Mode devices, including standard products with $V_{GS(th)}$ specified at -3.50V, -1.30V, -0.40V, +0.00V, +0.20V, +0.40V, +0.80V, +1.40V, and +3.30V. ALD can also provide any customer-desired $V_{GS(th)}$ between -3.50V and +3.50V on a special order basis. For all these devices ALD EPAD technology enables excellent well-controlled gate threshold voltage, subthreshold voltage, and low leakage characteristics. With well matched design and precision programming, units from different production lots provide the user with exceptional matching and uniformity characteristics. Built on the same monolithic IC chip, the units also have excellent temperature tracking characteristics.

This ALD2108xx/ALD2129xx/ALD2148xx/ALD2169xx EPAD MOSFET Array product family (EPAD MOSFET) is available in three separate categories, each providing a distinctly different set of electrical specifications and characteristics. The first category is the ALD210800A/ALD210800/ALD212900A/ALD212900 Zero-Threshold™ mode EPAD MOSFETs. The second is the ALD2108xx/ALD2129xx enhancement mode EPAD MOSFETs. The third category includes the ALD2148xx/ALD2169xx depletion mode EPAD MOSFETs. (The suffix “xx” denotes threshold voltage in 0.1V steps, for example, xx=08 denotes 0.80V). For each device, there is a zero-tempco bias current and bias voltage point. When a design utilizes such a feature, then the gate-threshold voltage is temperature stable, greatly simplifying certain designs where stability of certain circuit parameters over a temperature range is desired.

The ALD210800A/ALD210800 are quad Zero Threshold MOSFETs in which the individual gate-threshold voltage of each MOSFET is set at zero, $V_{GS(th)}$ = 0.00V at $I_{DS(ON)}$ = 10μA @ $V_{DS(ON)}$ = +0.1V ($I_{DS(ON)}$ = 20μA for the dual ALD212900A/ALD212900). Zero Threshold MOSFETs operate in the enhancement region when operated above threshold voltage (V_{GS} > 0.00V and I_{DS} > 10μA) and subthreshold region when operated at or below threshold voltage (V_{GS} ≤ 0.00V and I_{DS} < 10μA). These devices, along with other low $V_{GS(th)}$ members of the product family, enable ultra low supply voltage analog or digital operation and nanopower circuit designs, thereby reducing or eliminating the use of very high valued (expensive) resistors in many cases.

The ALD2108xx/ALD2129xx (quad/dual) product family features precision matched enhancement mode EPAD MOSFET devices, which require a positive gate bias voltage V_{GS} to turn on. Precision $V_{GS(th)}$ values at +3.30V, +1.40V, +0.80V, +0.40V and +0.20V are offered. No conductive channel exists between the source and drain at zero applied gate voltage (V_{GS} = 0.00V) for +3.30V, +1.40V and +0.80V versions. The +0.40V and the +0.20V versions have a subthreshold current at about 1nA and 100nA for the ALD2108xx (2nA and 200nA for the ALD2129xx) respectively at zero applied gate voltage. They are also capable of delivering lower $R_{DS(ON)}$ and higher output currents greater than 68mA (see specifications).

The ALD2148xx/ALD2169xx (quad/dual) features Depletion Mode EPAD MOSFETs, which are normally-on devices at zero applied gate voltage. The $V_{GS(th)}$ is set at a negative voltage level ($V- < V_{GS} < V_S$) at which the EPAD MOSFET turns off. Without a supply voltage and/or with V_{GS} = V- = 0.00V = Ground, the EPAD MOSFET device is already turned on and exhibits a defined and controlled on-resistance $R_{DS(ON)}$. An EPAD MOSFET may be turned off when a negative voltage is applied to V- pin and V_{GS} set more negative than its $V_{GS(th)}$. These Depletion Mode EPAD MOSFETs are different from most other depletion mode MOSFETs and JFETs in that they do not exhibit high gate leakage currents and channel/junction leakage currents, while they stay controlled, modulated and turned off at precise voltages. The same MOSFET device equations as those for enhancement mode devices apply.

KEY APPLICATION ENVIRONMENTS

EPAD MOSFETs are ideal for circuits requiring low V_{OS} and low operating currents with tracked differential thermal responses. They feature low input bias currents (less than 200pA max.), low input capacitance and fast switching speed. These and other operating characteristics offer unique solutions in one or more of the following operating environments:

* Low supply voltage: 0.1V to 10V (±0.05V to ±5V)
* Ultra low supply voltage: < ±10mV to ±0.1V
* Nanopower operation: voltage x current = nW or μW
* Precision V_{OS} characteristics
* Matching and tracking of multiple MOSFETs
* Matching across multiple packages

ELECTRICAL CHARACTERISTICS

The turn-on and turn-off electrical characteristics of the EPAD MOSFET products are shown in the $I_{DS(ON)}$ vs. $V_{DS(ON)}$ and $I_{DS(ON)}$ vs. V_{GS} graphs. Each graph shows $I_{DS(ON)}$ versus $V_{DS(ON)}$ characteristics as a function of V_{GS} in a different operating region under different bias conditions, while $I_{DS(ON)}$ at a given gate input voltage is controlled and predictable. A series of four graphs titled “Forward Transfer Characteristics”, with the 2nd and 3rd sub-titled “expanded (subthreshold)” and “further expanded (subthreshold)”, and the 4th sub-titled “low voltage”, illustrates the wide dynamic operating range of these devices.

Classic MOSFET equations for an N-channel MOSFET also apply to EPAD MOSFETs.

The drain current in the linear region ($V_{DS(ON)} < V_{GS} - V_{GS(th)}$) is given by:

$$I_{DS(ON)} = u \cdot C_{OX} \cdot W/L \cdot [V_{GS} - V_{GS(th)} - V_{DS}/2] \cdot V_{DS(ON)}$$

where:
- u = Mobility
- C_{OX} = Capacitance / unit area of Gate electrode
- V_{GS} = Gate to Source Voltage
- $V_{GS(th)}$ = Gate Threshold (Turn-on)Voltage
- $V_{DS(ON)}$ = Drain to Source On Voltage
- W = Channel width
- L = Channel length

In this region of operation the $I_{DS(ON)}$ value is proportional to the $V_{DS(ON)}$ value and the device can be used as a gate-voltage controlled resistor.

For higher values of $V_{DS(ON)}$ where $V_{DS(ON)} \geq V_{GS} - V_{GS(th)}$, the saturation current $I_{DS(ON)}$ is now given by (approx.):

$$I_{DS(ON)} = u \cdot C_{OX} \cdot W/L \cdot [V_{GS} - V_{GS(th)}]^2$$

PERFORMANCE CHARACTERISTICS OF EPAD®
PRECISION MATCHED PAIR MOSFET FAMILY (cont.)

SUB-THRESHOLD REGION OF OPERATION

The gate threshold (turn-on) voltage $V_{GS(th)}$ of the EPAD MOSFET is a voltage below which the MOSFET conduction channel rapidly turns off. For analog designs, this gate threshold voltage directly affects the operating signal voltage range and the operating bias current levels.

At a voltage below $V_{GS(th)}$, an EPAD MOSFET exhibits a turn-off characteristic in an operating region called the subthreshold region. This is when the EPAD MOSFET conduction channel rapidly turns off as a function of decreasing applied gate voltage. The conduction channel, induced by the gate voltage on the gate electrode, decreases exponentially and causes the drain current to decrease exponentially as well. However, the conduction channel does not shut off abruptly with decreasing gate voltage, but rather decreases at a fixed rate of about 104mV per decade of drain current decrease. For example, for the ALD2108xx device, if the gate threshold voltage is +0.20V, the drain current is 10μA at V_{GS} = +0.20V. At V_{GS} = +0.096V, the drain current would decrease to 1μA. Extrapolating from this, the drain current is about 0.1μA at V_{GS} = 0.00V, 1nA at V_{GS} = -0.216V, and so forth. This subthreshold characteristic extends all the way down to current levels below 1nA and is limited by junction leakage currents.

At a drain current of "zero current" as defined and selected by the user, the V_{GS} voltage at that zero current can now be estimated. Note that using the above example, with $V_{GS(th)}$ = +0.20V, the drain current still hovers around 100nA when the gate is at ground voltage. With a device that has $V_{GS(th)}$ = +0.40V (part number ALD210804), the drain current is about 2nA when the gate is at ground potential. Thus, in this case an input signal referenced to ground can operate with a natural drain current of only 2nA internal bias current, dissipating nano-watts of power.

LOW POWER AND NANOPOWER

When supply voltages decrease, the power consumption of a given load resistor decreases as the square of the supply voltage. Thus, one of the benefits in reducing supply voltage is to reduce power consumption. While decreasing power supply voltages and power consumption go hand-in-hand with decreasing useful AC bandwidth and increased noise effects in the circuit, a circuit designer can make the necessary tradeoffs and adjustments in any given circuit design and bias the circuit accordingly for optimal performance.

With EPAD MOSFETs, a circuit that performs any specific function can be designed so that power consumption of that circuit is minimized. These circuits operate in low power mode where the power consumed is measure in mW, μW, and nW (nano-watt) region and still provide a useful and controlled circuit function operation.

ZERO TEMPERATURE COEFFICIENT (ZTC) OPERATION

For an EPAD MOSFET in this product family, operating points exist where the various factors that cause the current to increase as a function of temperature balance out those that cause the current to decrease, thereby canceling each other, and resulting in a net temperature coefficient of near zero. An example of this temperature stable operating point is obtained by a ZTC voltage bias condition, which is 0.38V above $V_{GS(th)}$ when $V_{DS(ON)}$ = +0.1V, resulting in a temperature stable current level of about 380μA for the ALD2108xx and 760μA for the ALD2129xx devices.

PERFORMANCE CHARACTERISTICS

Performance characteristics of the EPAD MOSFET product family are shown in the following graphs. In general, the gate threshold voltage shift for each member of the product family causes other affected electrical characteristics to shift linearly with $V_{GS(th)}$ bias voltage. This linear shift in V_{GS} causes the subthreshold I-V curves to shift linearly as well. Accordingly, the subthreshold operating current can be determined by calculating the gate source voltage drop relative to its gate threshold voltage, $V_{GS(th)}$.

NORMALLY-ON FIXED $R_{DS(ON)}$ AT V_{GS} = GROUND

Several members of this MOSFET family produce a fixed resistance when their gate is grounded. For ALD210800, the drain current at V_{DS} = 0.1V is @ 10μA at V_{GS} = 0.00V. Thus, just by grounding the gate of the ALD210800, a resistor with $R_{DS(ON)}$ = ~10KΩ is produced (For ALD212900 device, $R_{DS(ON)}$ = ~5KΩ). When an ALD214804 gate is grounded, the drain current I_{DS} = 424μA @ V_{DS} = 0.1V, producing $R_{DS(ON)}$ = ~236Ω. Similarly, ALD214813 and ALD214835 produces 1.71mA and 3.33mA for each MOSFET, respectively, at V_{GS} = 0.00V, producing $R_{DS(ON)}$ values of 59Ω and 30Ω, respectively. For example, when all 4 MOSFETs in an ALD214835 are connected in parallel, an on-resistance of 30/4 = ~7.5Ω is measured between the Drain and Source terminals when V_{GS} = V- = 0.00V, producing a fixed on-resistance without any gate bias voltages applied to the device.

MATCHING CHARACTERISTICS

One of the key performance benefits of using matched-pair EPAD MOSFETs is to maintain temperature tracking between the different devices in the same package. In general, for EPAD MOSFET matched pair devices, one device of the matched pair has gate leakage currents, junction temperature effects, and drain current temperature coefficient as a function of bias voltage that cancel out similar effects of the other device, resulting in a temperature stable circuit. As mentioned earlier, this temperature stability can be further enhanced by biasing the matched-pairs at Zero Tempco (ZTC) point, even though that may require special circuit configurations and power consumption design considerations.

POWER SUPPLY SEQUENCES AND ESD CONTROL

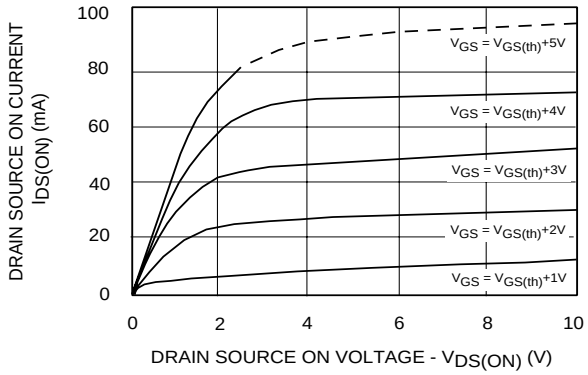
EPAD MOSFETs are robust and reliable, as demonstrated by more than a decade of production history supplied to a large installed base of customers across the world. However, these devices do require a few design and handling precautions in order for them to be used successfully.

EPAD MOSFETs, being a CMOS Integrated Circuit, in addition to having Drain, Gate and Source pins normally found in a MOSFET device, have three other types of pins, namely V+, V- and IC pins. V+ is connected to the substrate, which must always be connected to the most positive supply in a circuit. V- is the body of the MOSFET, which must be connected to the most negative supply voltage in the circuit. IC pins are internally connected pins, which must also be connected to V-. Drain, Gate and Source pins must have voltages between V- and V+ at all times.

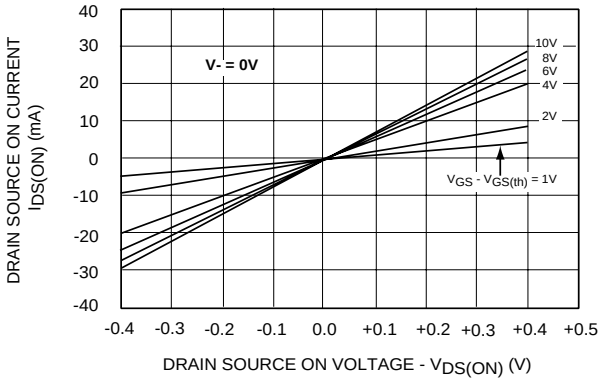
Proper power-up sequencing requires powering up supply voltages before applying any signals. During the power down cycle, remove all signals before removing V- and V+. This way internally back biased diodes are never allowed to become forward biased, possibly causing damage to the device. Of course, standard ESD control procedures should also be observed so that static charge does not degrade the performance of the devices.

TYPICAL PERFORMANCE CHARACTERISTICS

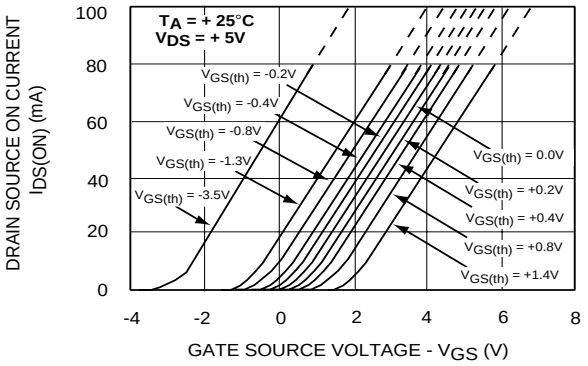
OUTPUT CHARACTERISTICS



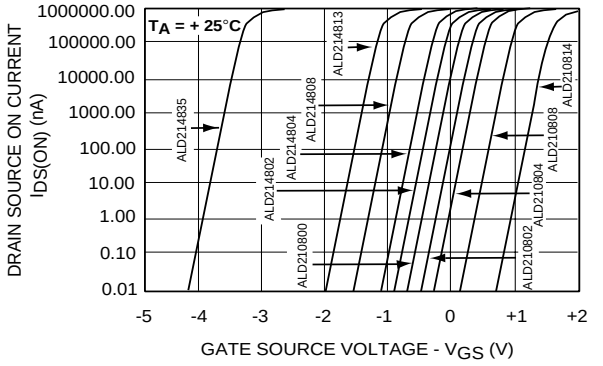
LOW VOLTAGE OUTPUT CHARACTERISTICS



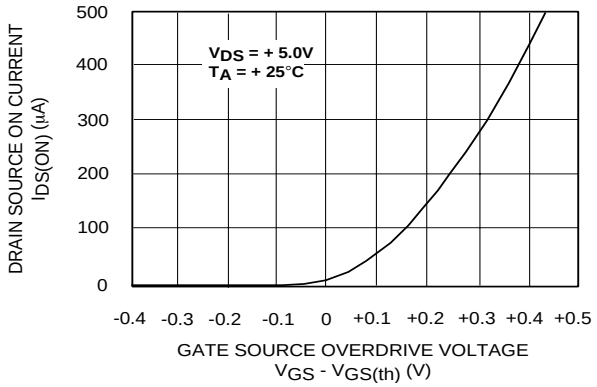
FORWARD TRANSFER CHARACTERISTICS



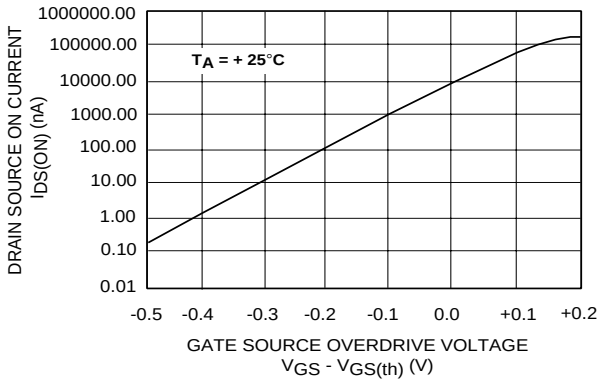
FORWARD TRANSFER CHARACTERISTICS EXPANDED (SUBTHRESHOLD)



FORWARD TRANSFER CHARACTERISTICS LOW VOLTAGE

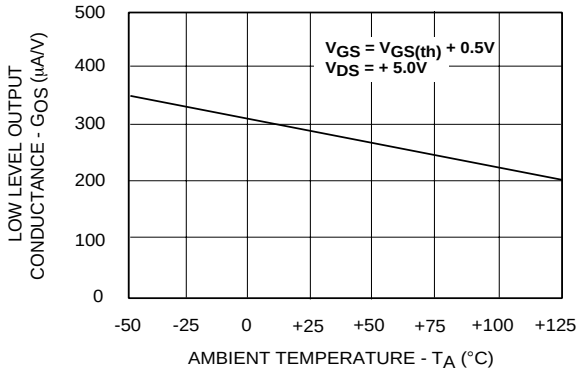


FORWARD TRANSFER CHARACTERISTICS FURTHER EXPANDED (SUBTHRESHOLD)

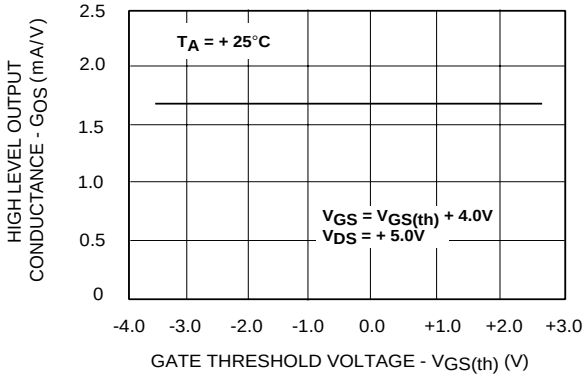


TYPICAL PERFORMANCE CHARACTERISTICS (cont.)

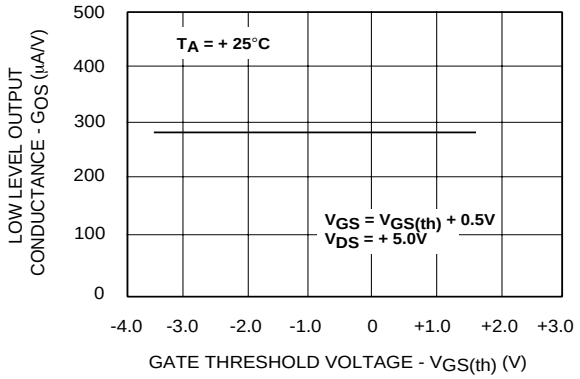
LOW LEVEL OUTPUT CONDUCTANCE vs. AMBIENT TEMPERATURE



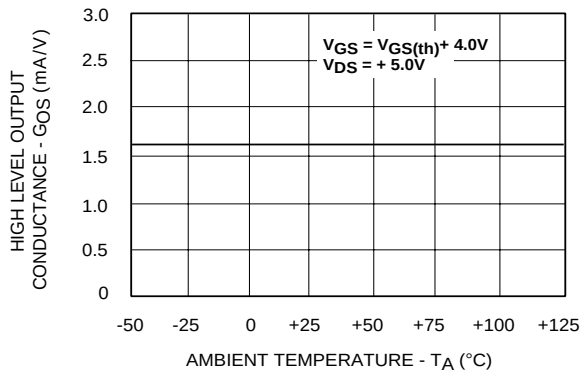
HIGH LEVEL OUTPUT CONDUCTANCE vs. GATE THRESHOLD VOLTAGE



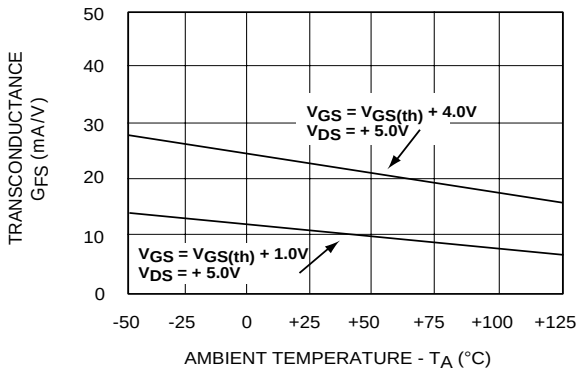
LOW LEVEL OUTPUT CONDUCTANCE vs. GATE THRESHOLD VOLTAGE



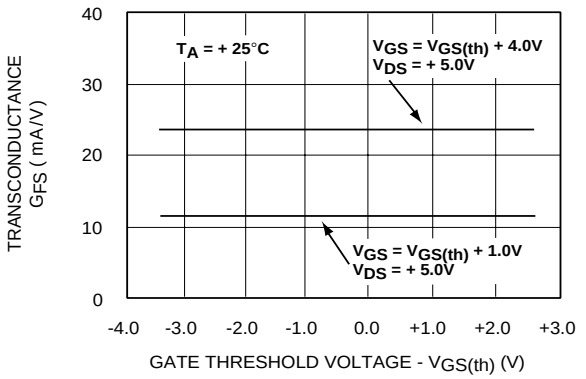
HIGH LEVEL OUTPUT CONDUCTANCE vs. AMBIENT TEMPERATURE



TRANSCONDUCTANCE vs. AMBIENT TEMPERATURE

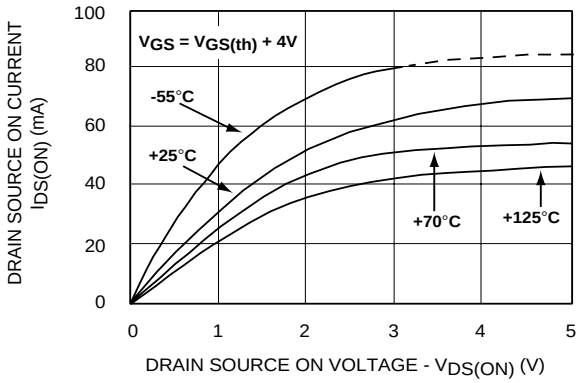


TRANSCONDUCTANCE vs. GATE THRESHOLD VOLTAGE

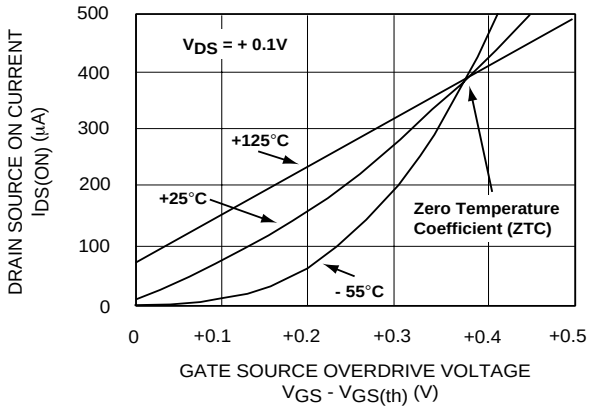


TYPICAL PERFORMANCE CHARACTERISTICS (cont.)

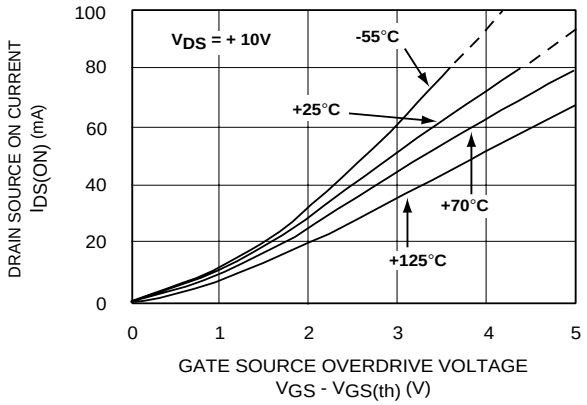
OUTPUT CHARACTERISTICS



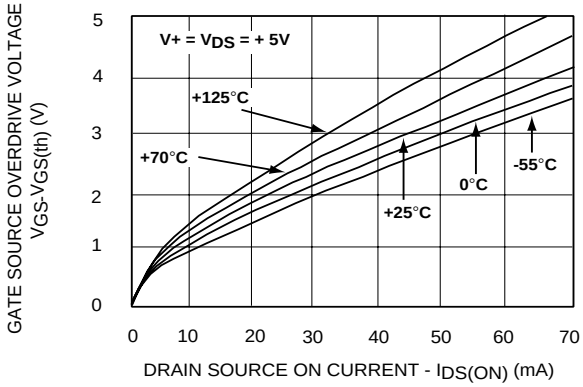
ZERO TEMPERATURE COEFFICIENT (ZTC)



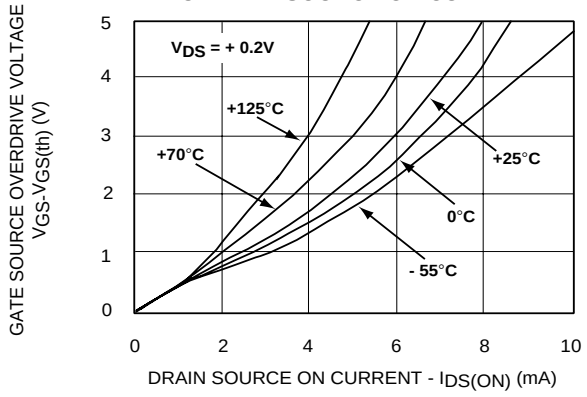
DRAIN SOURCE ON CURRENT vs. GATE SOURCE OVERDRIVE VOLTAGE



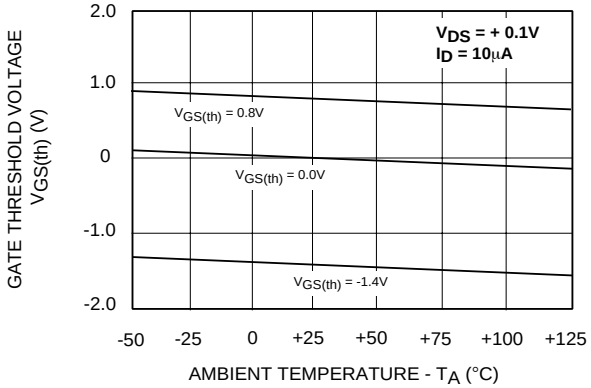
GATE SOURCE OVERDRIVE VOLTAGE vs. DRAIN SOURCE ON CURRENT



GATE SOURCE OVERDRIVE VOLTAGE vs. DRAIN SOURCE ON CURRENT

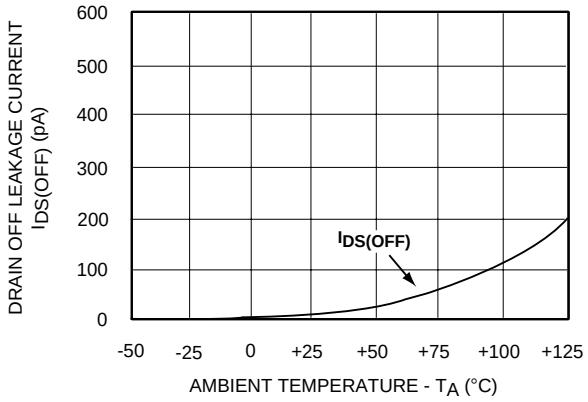


GATE THRESHOLD VOLTAGE vs. AMBIENT TEMPERATURE

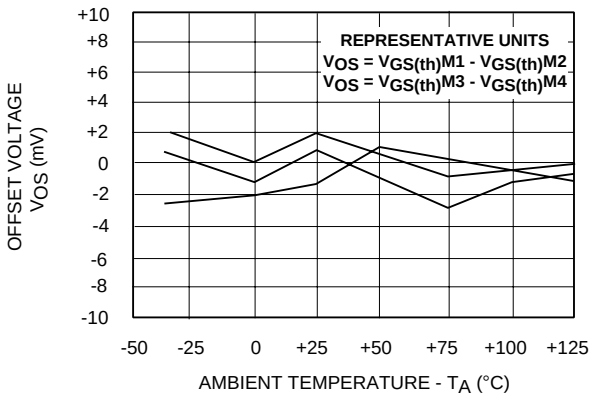


TYPICAL PERFORMANCE CHARACTERISTICS (cont.)

DRAIN OFF LEAKAGE CURRENT $I_{DS(OFF)}$ vs. AMBIENT TEMPERATURE

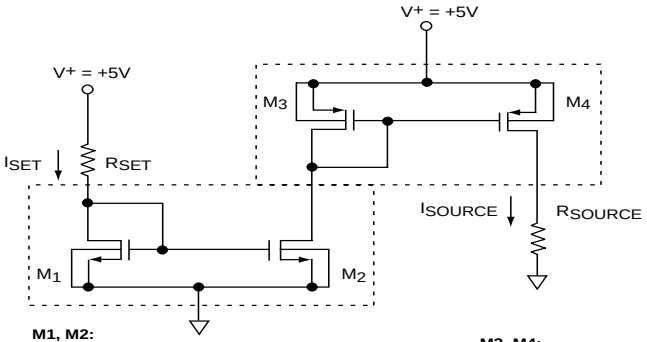


OFFSET VOLTAGE vs. AMBIENT TEMPERATURE



TYPICAL APPLICATIONS

CURRENT SOURCE MIRROR



M1, M2:
ALD1101,
ALD1116,
ALD1109xx,
ALD2129xx,
1/2 ALD1103,
1/2 ALD1105,
1/2 ALD1106,
1/2 ALD1108xx, or
1/2 ALD2108xx

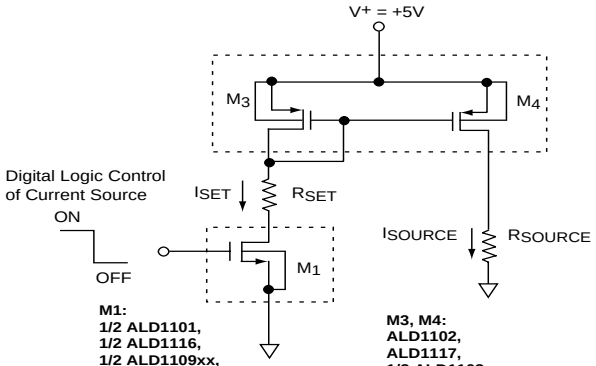
$$I_{SOURCE} = I_{SET} = \frac{V^+ - Vt}{R_{SET}}$$

where $Vt = V_{GS} - V_{GS(th)} = V_{DS}$

M3, M4:
ALD1102,
ALD1117,
1/2 ALD1103,
1/2 ALD1105,
1/2 ALD1107, or
1/2 ALD3107xx

M_1, M_2: N - Channel MOSFET
M_3, M_4: P - Channel MOSFET

CURRENT SOURCE WITH GATE CONTROL

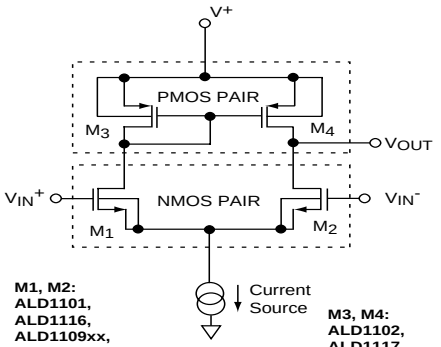


M1:
1/2 ALD1101,
1/2 ALD1116,
1/2 ALD1109xx,
1/2 ALD2129xx,
1/4 ALD1103,
1/4 ALD1105,
1/4 ALD1106,
1/4 ALD1108xx, or
1/4 ALD2108xx

M3, M4:
ALD1102,
ALD1117,
1/2 ALD1103,
1/2 ALD1105,
1/2 ALD1107, or
1/2 ALD3107xx

M_1 : N - Channel MOSFET
M_3, M_4 : P - Channel MOSFET

DIFFERENTIAL AMPLIFIER

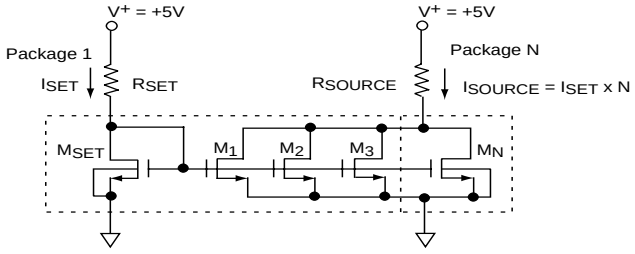


M1, M2:
ALD1101,
ALD1116,
ALD1109xx,
ALD2129xx,
1/2 ALD1103,
1/2 ALD1105,
1/2 ALD1106,
1/2 ALD1108xx, or
1/2 ALD2108xx

M3, M4:
ALD1102,
ALD1117,
1/2 ALD1103,
1/2 ALD1105,
1/2 ALD1107, or
1/2 ALD3107xx

M_1, M_2: N - Channel MOSFET
M_3, M_4: P - Channel MOSFET

CURRENT SOURCE MULTIPLICATION



MSET, M1..MN:
N x ALD1101, N x ALD1116,
N x ALD1109xx, N x ALD2129xx,
N x ALD1103, N x ALD1106,
N x ALD1108xx, or
N x ALD2108xx

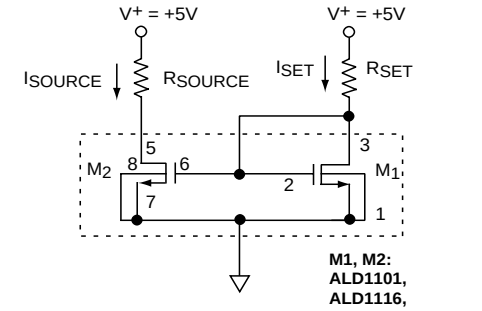
All M's in the set are
from the same part number.

M_{SET}, M_1..M_N: N - Channel MOSFET

TYPICAL APPLICATIONS (cont.)

BASIC CURRENT SOURCES

N- CHANNEL CURRENT SOURCE



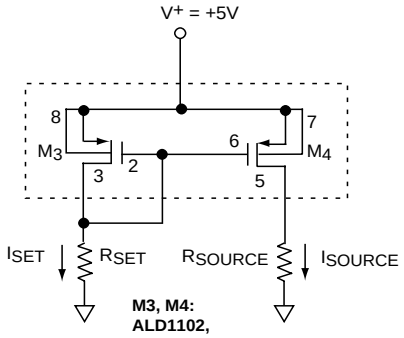
$I_{SOURCE} = I_{SET} = \frac{V^+ - Vt}{R_{SET}}$

where $Vt = V_{GS} - V_{GS(th)} = V_{DS}$

M1, M2:
ALD1101,
ALD1116,
ALD1109xx,
ALD2129xx,
1/2 ALD1103,
1/2 ALD1105,
1/2 ALD1106,
1/2 ALD1108xx, or
1/2 ALD2108xx

M_1, M_2 :N - Channel MOSFET

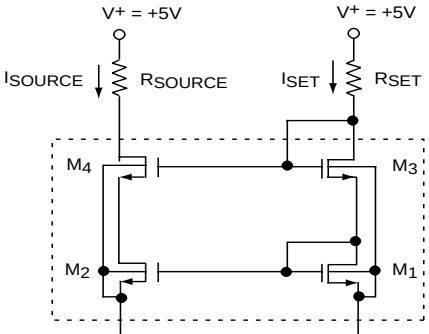
P- CHANNEL CURRENT SOURCE



M3, M4:
ALD1102,
ALD1117,
1/2 ALD1103,
1/2 ALD1105,
1/2 ALD1107, or
1/2 ALD3107xx

M_3, M_4: P - Channel MOSFET

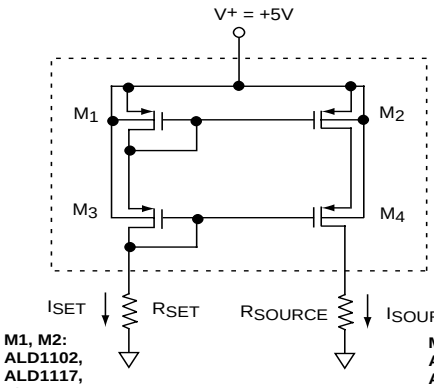
CASCODE CURRENT SOURCES



M1, M2:
ALD1101,
ALD1116,
ALD2129xx,
1/2 ALD1103,
1/2 ALD1105,
1/2 ALD1106, or
1/2 ALD2108xx

M3, M4:
ALD1101,
ALD1116,
1/2 ALD1103,
1/2 ALD1105,
1/2 ALD1106, or
1/2 ALD2108xx

M_1, M_2, M_3, M_4: N - Channel MOSFET
where M1 and M2 is a matched pair
and M3 and M4 is a second matched pair.



M1, M2:
ALD1102,
ALD1117,
1/2 ALD1103,
1/2 ALD1105,
1/2 ALD1107, or
1/2 ALD3107xx

$I_{SOURCE} = I_{SET} = \frac{V^+ - 2Vt}{R_{SET}}$

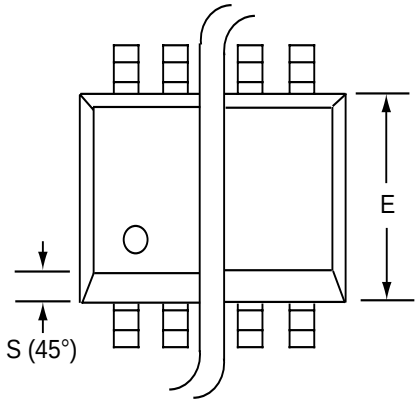
where $Vt = V_{GS} - V_{GS(th)} = V_{DS}$

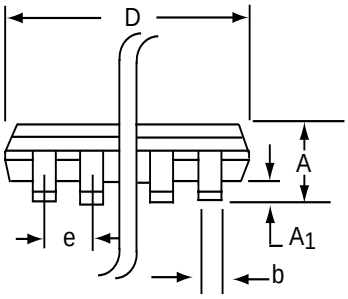
M3, M4:
ALD1102,
ALD1117,
1/2 ALD1103,
1/2 ALD1105,
1/2 ALD1107, or
1/2 ALD3107xx

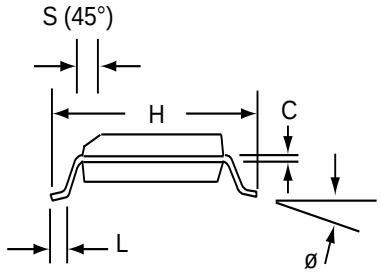
M_1, M_2, M_3, M_4: P - Channel MOSFET
where M1 and M2 is a matched pair
and M3 and M4 is a second matched pair.

SOIC-16 PACKAGE DRAWING

16 Pin Plastic SOIC Package



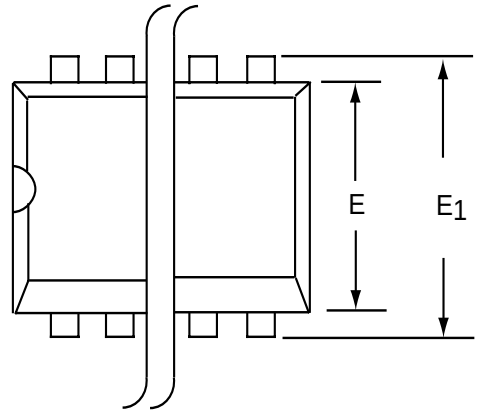


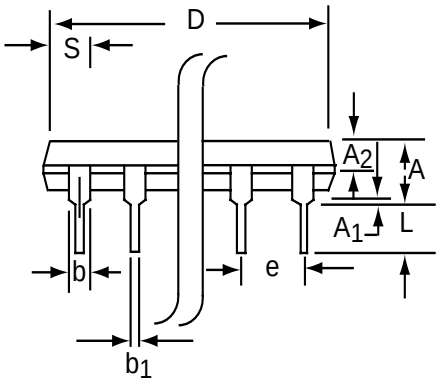


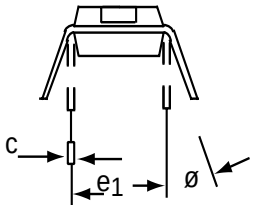
Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A_1	0.10	0.25	0.004	0.010
b	0.35	0.45	0.014	0.018
C	0.18	0.25	0.007	0.010
D-16	9.80	10.00	0.385	0.394
E	3.50	4.05	0.140	0.160
e	1.27 BSC		0.050 BSC	
H	5.70	6.30	0.224	0.248
L	0.60	0.937	0.024	0.037
Ø	0°	8°	0°	8°
S	0.25	0.50	0.010	0.020

PDIP-16 PACKAGE DRAWING

16 Pin Plastic DIP Package







Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	3.81	5.08	0.105	0.200
A_1	0.38	1.27	0.015	0.050
A_2	1.27	2.03	0.050	0.080
b	0.89	1.65	0.035	0.065
b_1	0.38	0.51	0.015	0.020
c	0.20	0.30	0.008	0.012
D-16	18.93	21.33	0.745	0.840
E	5.59	7.11	0.220	0.280
E_1	7.62	8.26	0.300	0.325
e	2.29	2.79	0.090	0.110
e_1	7.37	7.87	0.290	0.310
L	2.79	3.81	0.110	0.150
S-16	0.38	1.52	0.015	0.060
ø	0°	15°	0°	15°