NB3N502DEVB

NB3N502DEVB Evaluation Board User's Manual

ON Semiconductor®

http://onsemi.com

EVAL BOARD USER'S MANUAL

Description

The NB3N502 Evaluation Board was designed to provide a flexible and convenient platform to quickly evaluate, characterize and verify the performance and operation of the NB3N502 PLL Clock Multiplier. This user's manual provides detailed information on the board's contents, layout and use, and it should be used in conjunction with the NB3N502 data sheet which contains full technical details on device specifications and operation (www.onsemi.com).

Board Features

- Fully Assembled Evaluation Board
- Accommodates the Electrical Characterization of the NB3N502 in the SOIC−8 Package
- Supports the Use of a 5 MHz to 27 MHz Through−hole or Surface Mount Crystal
- SMA Connectors are Provided for Auxiliary Input and Output Interfaces
- Incorporates Onboard Slide Switch Controlled Multiplier Select Pins, Minimizing Excess Cabling

This Evaluation Board Manual Contains

- Information on the NB3N502 Evaluation Board
- Appropriate Lab Setup
- Evaluation Board Layout
- Bill of Materials

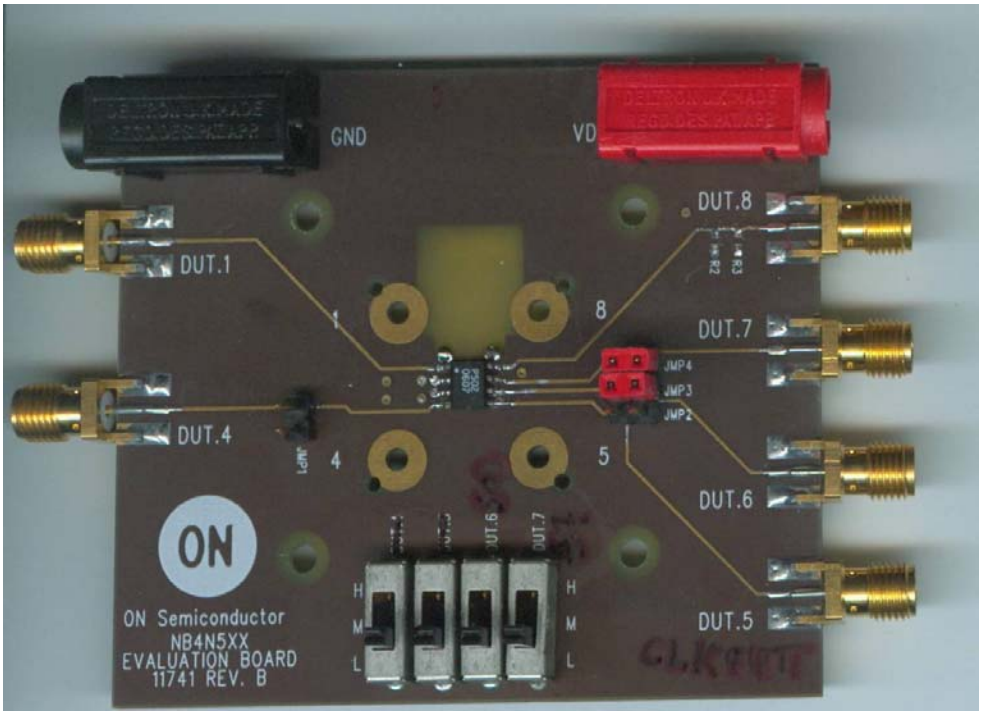

Figure 1. NB3N502 Evaluation Board

SETUP FOR MEASUREMENTS

Basic Equipment

- Signal Generator (for External Reference Clock Input)
- Oscilloscope
- Power Supply
- Voltmeter
- High−Speed Cables with SMA Connectors
- High−Impedance Probe

Power Supply Connections

External power supply of +3 V to +5.5 V must be provided to the board.

The NB4N502 has a positive supply pin, V_{DD}, and a ground pin, GND. Connect a single power supply to the evaluation board (see Figure 2.) by connecting V_{DD} to the positive supply, +3 V to +5.5 V, and GND to 0 V. Power supply banana plug connectors for V_{DD} and GND are provided at the top corners of the board.

Table 1. POWER SUPPLY CONNECTIONS

Supply	Value	Connector
V_{DD}	+3 to +5.5 V	Red Banana Plug
GND	0 V	Black Banana Plug

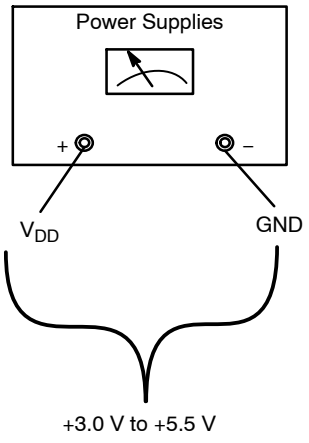

Figure 2. Power Supply Connections

External Reference Clock

An SMA connector is provided for X1/CLK if an external clock source is used on Pin 1. The metal trace at the package pin is intentionally open for crystal use and must be shorted for a connection to Pin 1 for external clock use.

Crystal and Crystal Load Capacitors Selection Guide

A through−hole or surface mount crystal can be used. The metal traces at the crystal pins are intentionally open for crystal use and will have no impedance effect on the crystal pins.

The total on−chip capacitance is approximately 12 pF per pin (CIN1 and CIN2). A parallel resonant, fundamental mode crystal should be used. The evaluation board includes pads for small capacitors from X1/CLK to ground and from X2 to ground. These capacitors, CL1 and CL2, are used to adjust the stray capacitance of the board to match the nominally required crystal load capacitance (CLOAD (crystal)). Crystal load capacitors must be connected from each of the pins X1 and X2 to ground. The load capacitance of the crystal (CLOAD (crystal)) must be matched by total load capacitance of the oscillator circuitry network, CINX, CSX and CLX, as seen by the crystal (see Figure 3 and equations below).

CLOAD1 = CIN1 + CS1 + CL1
[Total capacitance on X1/CLK]

CLOAD2 = CIN2 + CS2 + CL2 [Total capacitance on X2]

CIN1 ≈ CIN2 ≈ 12 pF (Typ) [Internal capacitance]

CS1 ≈ CS2 ≈ 5 pF (Typ) [External PCB stray capacitance]

CLOAD1,2 = 2 – CLOAD (Crystal)

CL2 = CLOAD2 − CIN2 − CS2
[External load capacitance on X2]

CL1 = CLOAD1 − CIN1 − CS1
[External load capacitance on X1/CLK]

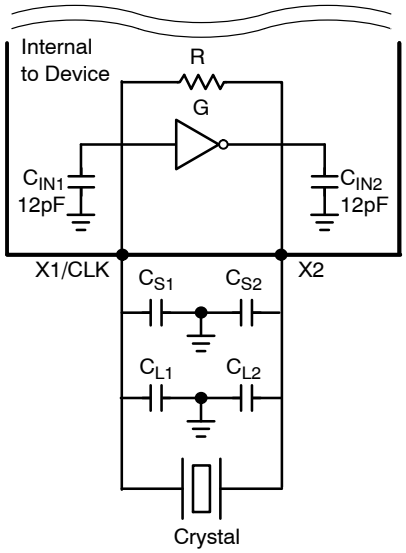

Figure 3. Using a Crystal as Reference Clock

Control and Select Pins

The NB4N502 evaluation board is equipped with SMA connectors to control the static input logic levels of the Multiplier Select pins, S0 and S1 (see Table 2).

Pin S1 defaults to M when left open. Pin S0 defaults to H when left open.

3−Position slide switches are also provided to control the Multiplier Select pins. To use the switches, headers JMP3 and JMP4 must be shorted.

1. **Using the SMA Connectors**
   a. SMA connectors J3 and J4 (DUT.6 and DUT.7) should be pulled to V_{CC} for logic level HIGH, pulled to GND for logic level LOW, and left OPEN for logic level M.
2. **Using the Slide Switches**
   a. Header pins JMP3 and JMP4 enable the slide switches for the clock multiplier select lines, S0 and S1, and should be jumpered.
   b. Switches SW3 (DUT.6) and SW4 (DUT.7) are used to select the clock multiplier value (see Table 2).
   c. The H position of the slide switch asserts a logic HIGH on the assigned pin, the L asserts a logic LOW and the M is an open where the pin "floats" to a mid−logic level by way of the device's internal pullup and pulldown resistors.

Table 2. CLOCK MULTIPLIER SELECT TABLE

S1* SW4 (DUT.7)	S0** SW3 (DUT.6)	Multiplier
L	L	2X
L	H	5X
M	L	3X
M	H	3.33X
H	L	4X
H	H	2.5X

L = GND, H = V_{DD}, M = OPEN (unconnected)
*Pin S1 defaults to M when left open
** Pin S0 defaults to H when left open

Table 3. HEADER PIN CONDITIONS

Header	Slide Switch Multiplier Control	SMA Multiplier Control
JMP1	Open	Open
JMP2	Open	Open
JMP3	Jumper (Short Pins)	Open
JMP4	Jumper (Short Pins)	Open

Output Connections

Connect the CMOS/TTL outputs, REF and CLKOUT, to the oscilloscope.

Table 4. OUTPUT CONNECTORS

Outputs	Board Connector
REF	J1 (DUT.4)
CLKOUT	J2 (DUT.5)

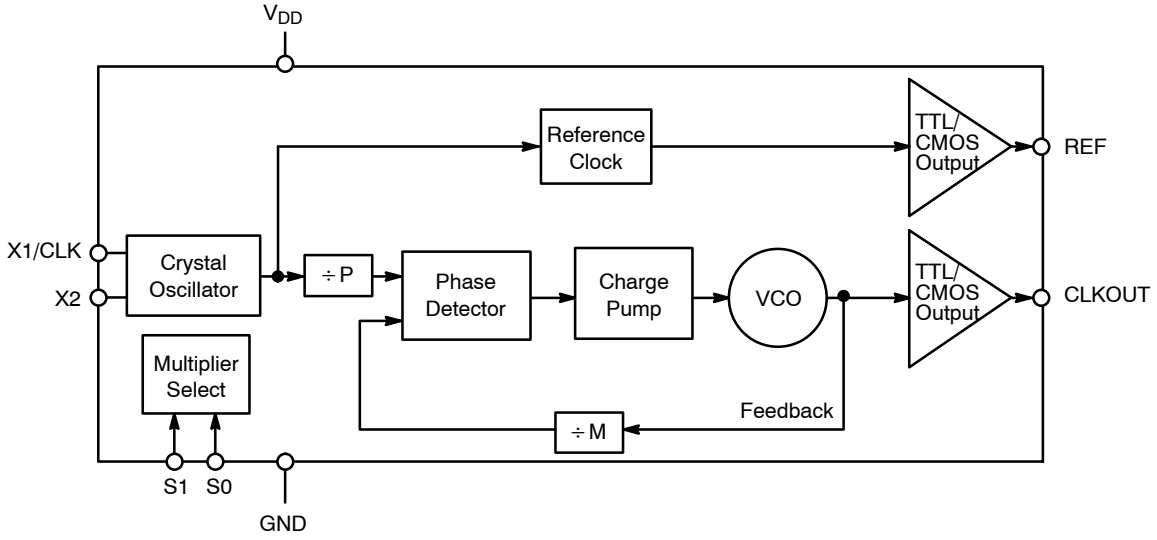

Figure 4. NB3N502 Logic Diagram

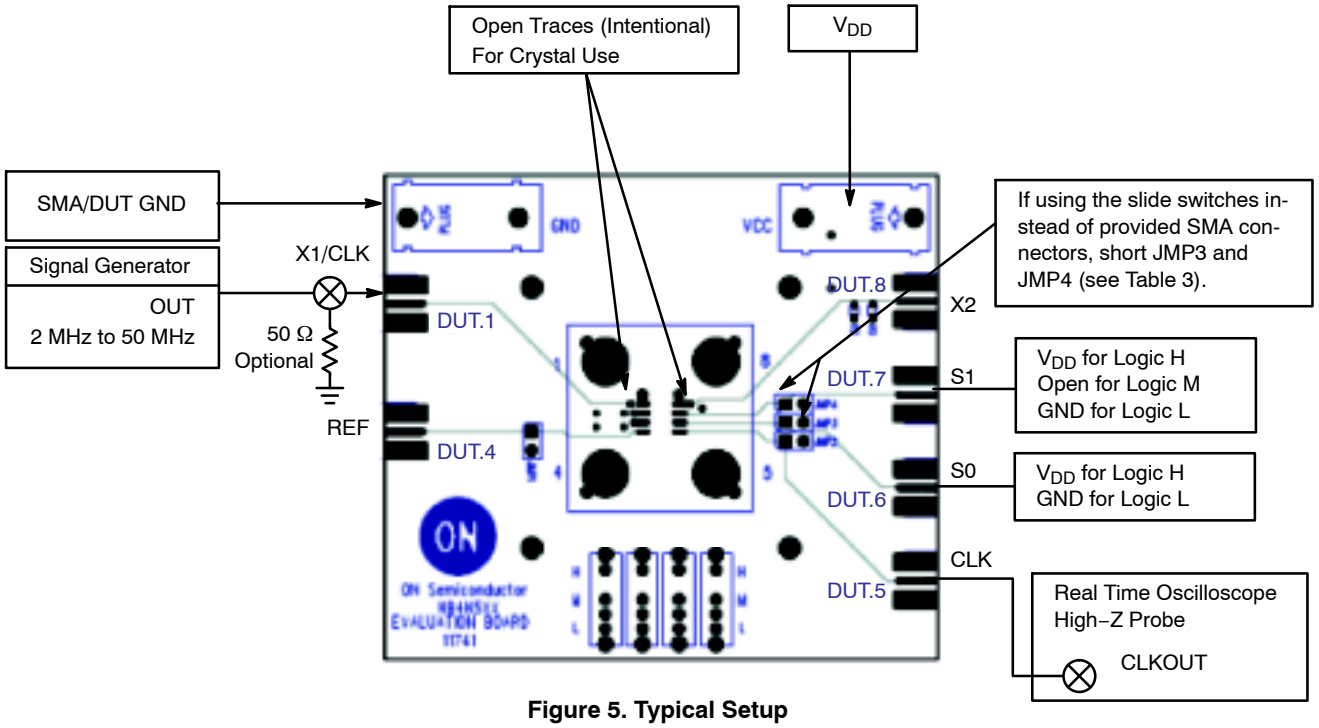

Figure 5. Typical Setup

Table 5. PARTS LIST

Ref. Number	Qty	Description	Manufacturer (Notes 1 and 2)
R1	1	Not populated	
R2	1	Not populated	
R3	1	Not populated	
C1	1	Not populated	
C2	1	Not populated	
C9	1	22 μF ± 10%, Size “C” Tantalum Capacitor, T494C226K016AT	KEMET
C10	1	0.01 μF ± 10%, (0603), Ceramic Capacitors, 06035C103KAT2A	AVX
C11	1	0.1 μF ± 10%, (0603), Ceramic Capacitors, 06035C104KAT2A	AVX
Y1	1	25 MHz Crystal	
U1	1	NB3N502, 8 pin SOIC (Pb−Free)	ON Semiconductor
SW1 − SW4	4	Slide Switches, 3 Position Miniature, OS103011MS8QP1	C&K
J1 − J6	6	SMA Edge Mount Connectors, 142−0711−821	Johnson
JMP1−JMP4	4	Jumper Header, 100 mil, 2 pins, 1 row, SPC20485	SPC
V_{DD} Plug	1	Banana Plug, Red, 571−0500	Deltron
GND Plug	1	Banana Plug, Black, 571−0100	Deltron

1. Specified parts are RoHS Compliant.
2. Only RoHS compliant parts may be substituted.

BOARD LAYOUT

The evaluation board is constructed with Getek material with 50 Ω trace impedances and is designed to minimize noise, achieve high bandwidth and minimize crosstalk.

Layer Stack
L1 Signal
L2 Ground
L3 V_{DD}
L4 Signal

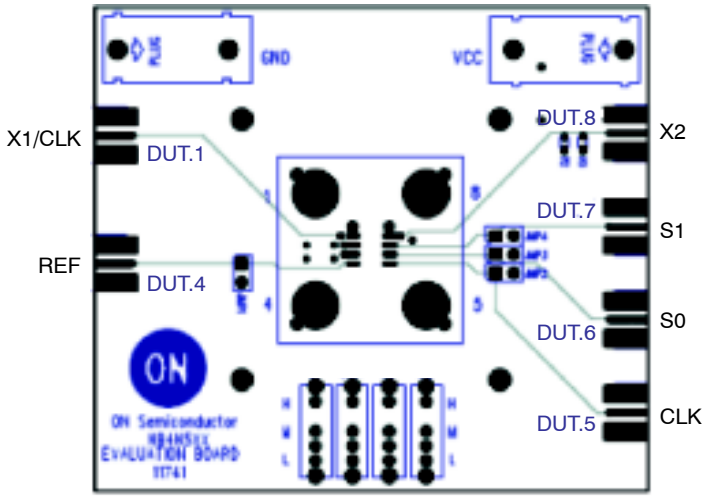

Figure 6. NB3N502 Evaluation Board Top (Component) Layer

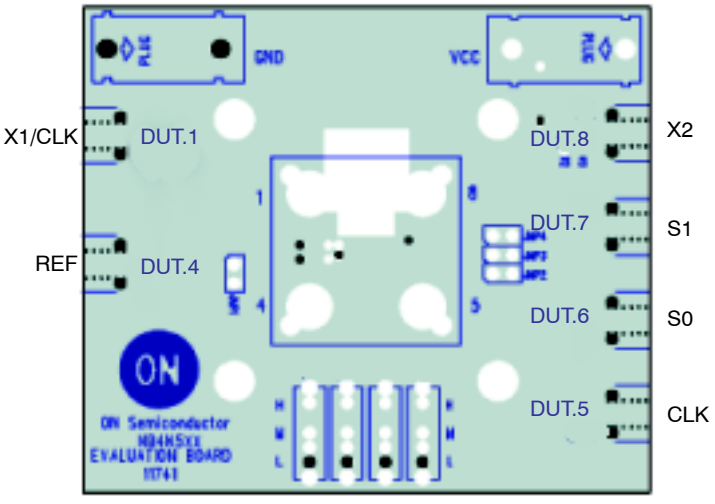

Figure 7. NB3N502 Evaluation Board SMA – Ground Layer

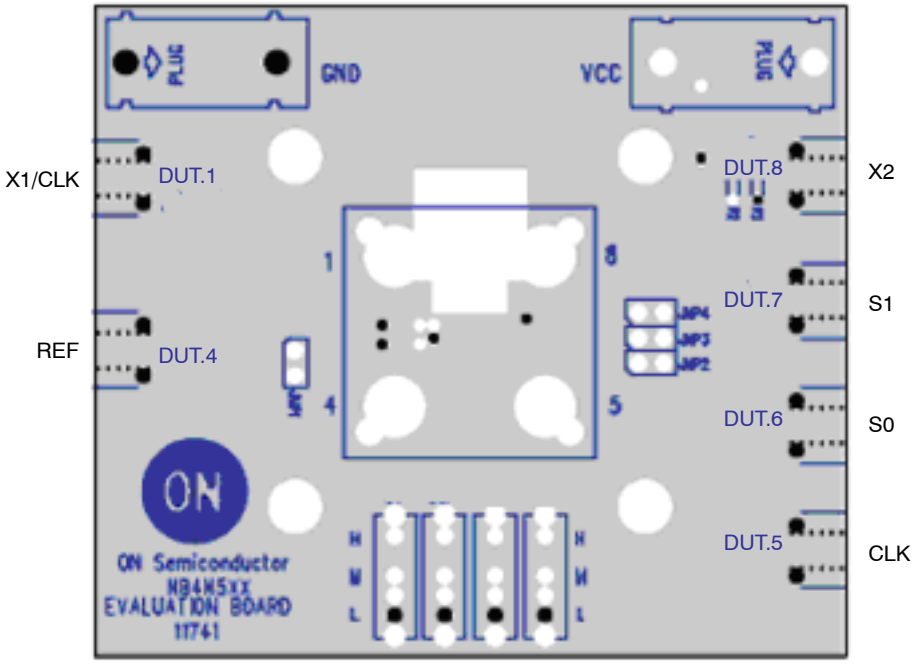

Figure 8. NB3N502 Evaluation Board Power Layer

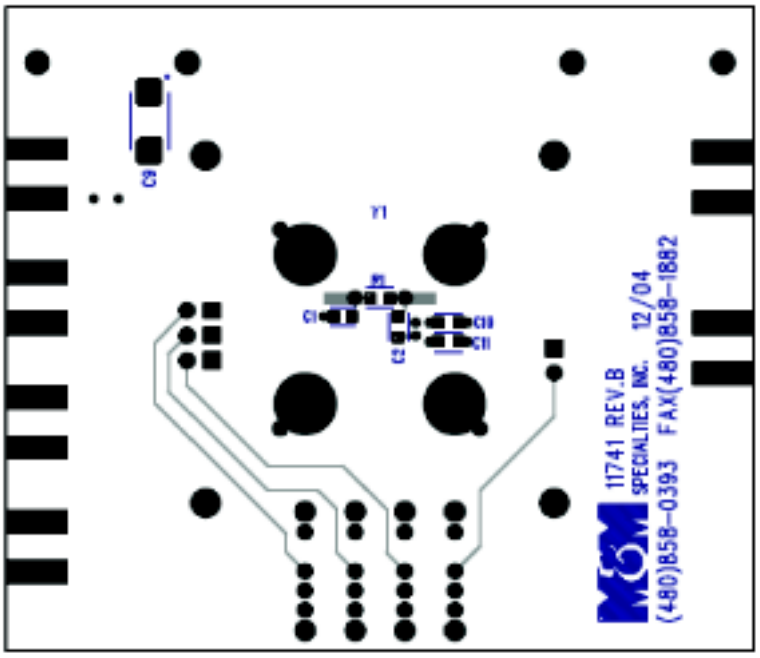

Figure 9. NB3N502 Evaluation Board Bottom Layer

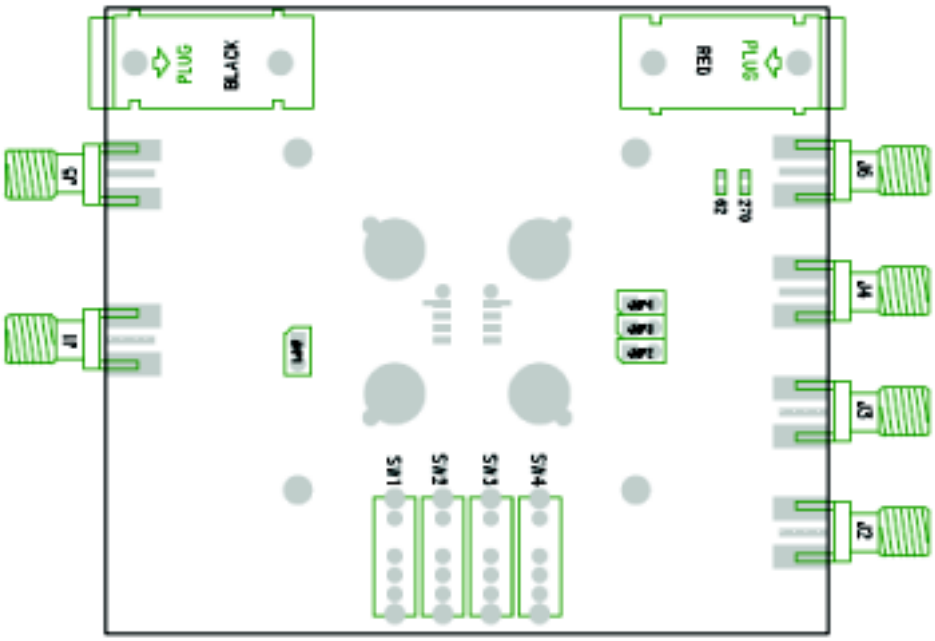

Figure 10. NB3N502 Evaluation Board Top Assembly

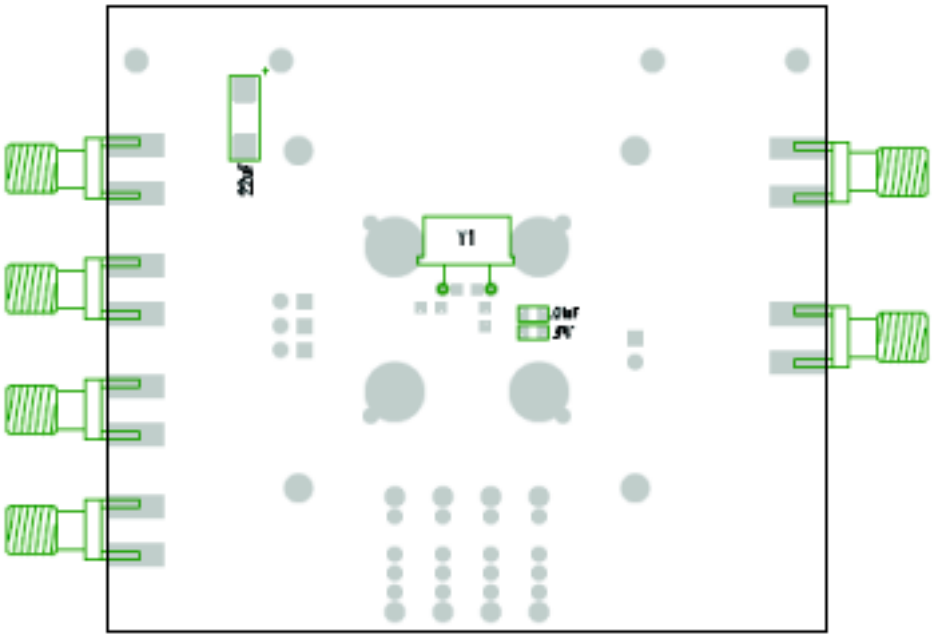

Figure 11. NB3N502 Evaluation Board Bottom Assembly

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5817−1050

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative

EVBUM2064/D