Freescale Semiconductor
Technical Data

RF Power Field Effect Transistor
N–Channel Enhancement–Mode Lateral MOSFET

Designed for CDMA base station applications with frequencies from 1930 to 1990 MHz. Can be used in Class AB and Class C for all typical cellular base station modulation formats.

- Typical Single–Carrier W–CDMA Performance: V_{DD} = 28 Volts, I_{DQ} = 1200 mA, P_{out} = 36 Watts Avg., f = 1990 MHz, IQ Magnitude Clipping, Channel Bandwidth = 3.84 MHz, Input Signal PAR = 7.5 dB @ 0.01% Probability on CCDF.
  Power Gain — 18 dB
  Drain Efficiency — 32%
  Device Output Signal PAR — 6.1 dB @ 0.01% Probability on CCDF
  ACPR @ 5 MHz Offset — –38.5 dBc in 3.84 MHz Channel Bandwidth
- Capable of Handling 10:1 VSWR, @ 32 Vdc, 1960 MHz, 120 Watts CW Output Power
- P_{out} @ 1 dB Compression Point $\simeq$ 120 W CW

Features

- 100% PAR Tested for Guaranteed Output Power Capability
- Characterized with Series Equivalent Large–Signal Impedance Parameters
- Internally Matched for Ease of Use
- Integrated ESD Protection
- Greater Negative Gate–Source Voltage Range for Improved Class C Operation
- Designed for Digital Predistortion Error Correction Systems
- 225°C Capable Plastic Package
- RoHS Compliant
- In Tape and Reel. R1 Suffix = 500 Units, 44 mm Tape Width, 13 inch Reel.

MRF7S19120NR1

1930–1990 MHz, 36 W AVG., 28 V SINGLE W–CDMA LATERAL N–CHANNEL RF POWER MOSFET
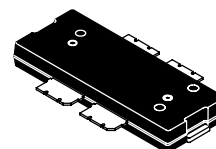
**CASE 1730–02
TO–270 WBL–4
PLASTIC**

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	–0.5, +65	Vdc
Gate–Source Voltage	V_{GS}	–6.0, +10	Vdc
Operating Voltage	V_{DD}	32, +0	Vdc
Storage Temperature Range	T_{stg}	– 65 to +150	°C
Case Operating Temperature	T_C	150	°C
Operating Junction Temperature [1,2]	T_J	225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value [2,3]	Unit

Thermal Resistance, Junction to Case
    Case Temperature 81°C, 120 W CW
    Case Temperature 80°C, 36 W CW
	$R_{\theta JC}$	
		0.43
		0.51
			°C/W

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at http://www.freescale.com/rf. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.freescale.com/rf. Select Documentation/Application Notes – AN1955.

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Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22–A114)	2 (Minimum)
Machine Model (per EIA/JESD22–A115)	A (Minimum)
Charge Device Model (per JESD22–C101)	III (Minimum)

Table 4. Moisture Sensitivity Level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD22–A113, IPC/JEDEC J–STD–020	3	260	°C

Table 5. Electrical Characteristics (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate–Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
On Characteristics					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 270 μAdc)	$V_{GS(th)}$	1.2	2	2.7	Vdc
Gate Quiescent Voltage (V_{DD} = 28 Vdc, I_D = 1200 mAdc, Measured in Functional Test)	$V_{GS(Q)}$	2	2.7	3.5	Vdc
Drain–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 2.7 Adc)	$V_{DS(on)}$	0.15	0.275	0.35	Vdc
Dynamic Characteristics [1]					
Reverse Transfer Capacitance (V_{DS} = 28 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{rss}	—	1.65	—	pF
Output Capacitance (V_{DS} = 28 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{oss}	—	600	—	pF
Input Capacitance (V_{DS} = 28 Vdc, V_{GS} = 0 Vdc ± 30 mV(rms)ac @ 1 MHz)	C_{iss}	—	1.03	—	pF

Functional Tests (In Freescale Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ} = 1200 mA, P_{out} = 36 W Avg., f = 1990 MHz, Single–Carrier W–CDMA, IQ Magnitude Clipping, Input Signal PAR = 7.5 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset.

Power Gain	G_{ps}	16.5	18	19.5	dB
Drain Efficiency	η_D	30	32	36	%
Output Peak–to–Average Ratio @ 0.01% Probability on CCDF	PAR	5.7	6.1	—	dB
Adjacent Channel Power Ratio	ACPR	—	–38.5	–35.5	dBc
Input Return Loss	IRL	—	–10	–7	dB

1. Part internally matched both on input and output.

Table 5. Electrical Characteristics (T$_A$ = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Typical Performances (In Freescale Test Fixture, 50 ohm system) V$_{DD}$ = 28 Vdc, I$_{DQ}$ = 1200 mA, 1930–1990 MHz Bandwidth					
Video Bandwidth @ 120 W PEP P$_{out}$ where IM3 = –30 dBc (Tone Spacing from 100 kHz to VBW) ΔIMD3 = IMD3 @ VBW frequency – IMD3 @ 100 kHz <1 dBc (both sidebands)	VBW	—	20	—	MHz
Gain Flatness in 60 MHz Bandwidth @ P$_{out}$ = 36 W Avg.	G$_F$	—	0.495	—	dB
Average Deviation from Linear Phase in 60 MHz Bandwidth @ P$_{out}$ = 120 W CW	Φ	—	0.914	—	°
Average Group Delay @ P$_{out}$ = 120 W CW, f = 1960 MHz	Delay	—	1.98	—	ns
Part–to–Part Insertion Phase Variation @ P$_{out}$ = 120 W CW, f = 1960 MHz, Six Sigma Window	ΔΦ	—	33.9	—	°
Gain Variation over Temperature (–30°C to +85°C)	ΔG	—	0.016	—	dB/°C
Output Power Variation over Temperature (–30°C to +85°C)	ΔP1dB	—	0.009	—	dB/°C

MRF7S19120NR1
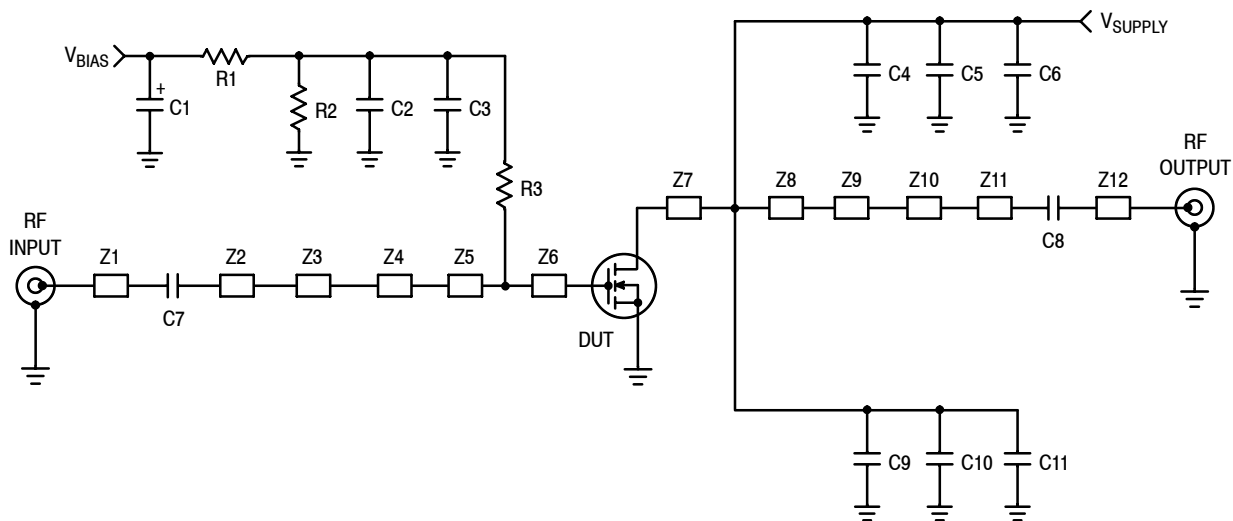
Z1	0.084″ x 0.744″ Microstrip	Z8	0.880″ x 0.210″ Microstrip
Z2	0.084″ x 0.797″ Microstrip	Z9	0.730″ x 0.350″ Microstrip
Z3	0.362″ x 0.100″ Microstrip	Z10	0.440″ x 0.130″ Microstrip
Z4	0.612″ x 0.380″ Microstrip	Z11	0.084″ x 0.700″ Microstrip
Z5	1.000″ x 0.125″ Microstrip	Z12	0.084″ x 0.743″ Microstrip
Z6	1.000″ x 0.090″ Microstrip	PCB	Arlon CuClad 250GX–0300–55–22, 0.030″, $\varepsilon_r = 2.55$
Z7	0.880″ x 0.111″ Microstrip		

Figure 1. MRF7S19120NR1 Test Circuit Schematic

Table 6. MRF7S19120NR1 Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1	10 µF, 35 V Tantalum Capacitor	T491D106K035AT	Kemet
C2	0.01 µF Chip Capacitor	C1825C103J1GAC	Kemet
C3, C4, C8, C9	5.1 pF Chip Capacitors	ATC100B5R1BT500XT	ATC
C5, C6, C10, C11	10 µF Chip Capacitors	GRM55DR61H106KA88L	Murata
C7	11 pF Chip Capacitor	ATC100B110BT500XT	ATC
R1	1 KΩ, 1/4 W Chip Resistor	CRCW12061001FKEA	Vishay
R2	10 KΩ, 1/4 W Chip Resistor	CRCW12061002FKEA	Vishay
R3	10 Ω, 1/4 W Chip Resistor	CRCW120610R0FKEA	Vishay
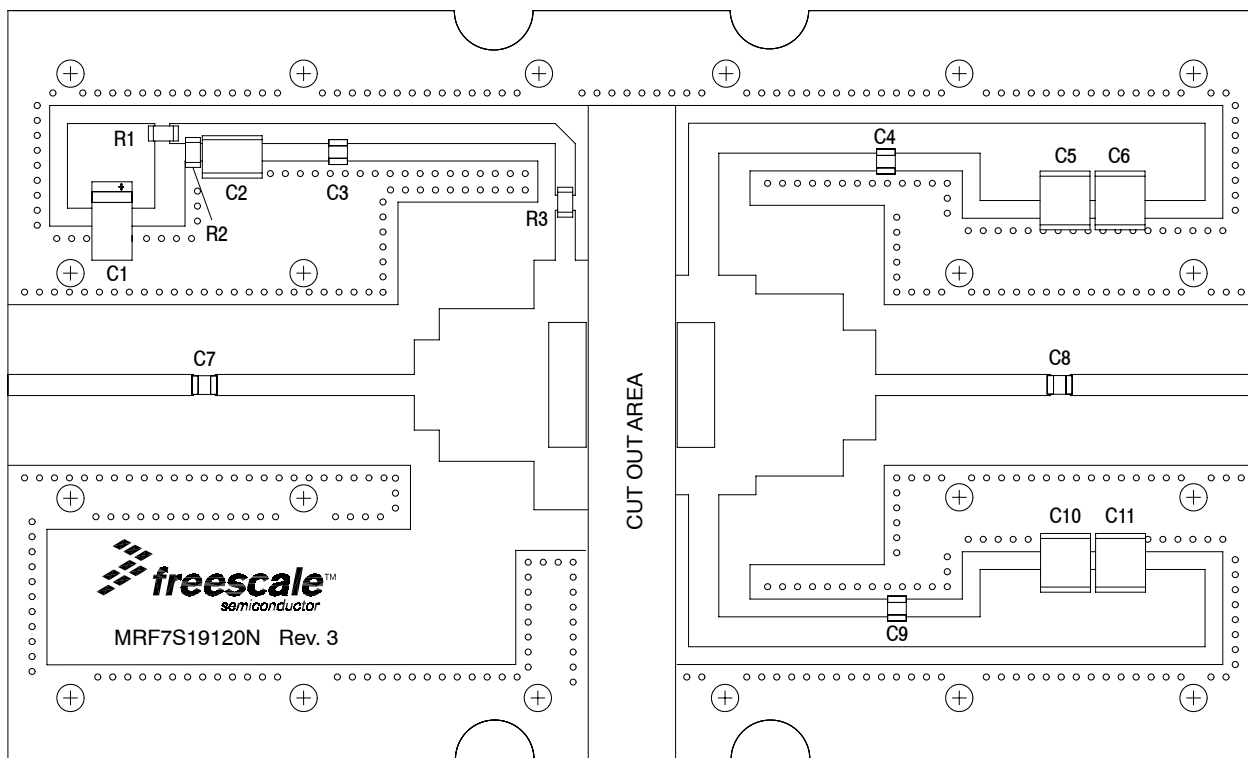
MRF7S19120NR1

Figure 2. MRF7S19120NR1 Test Circuit Component Layout

TYPICAL CHARACTERISTICS
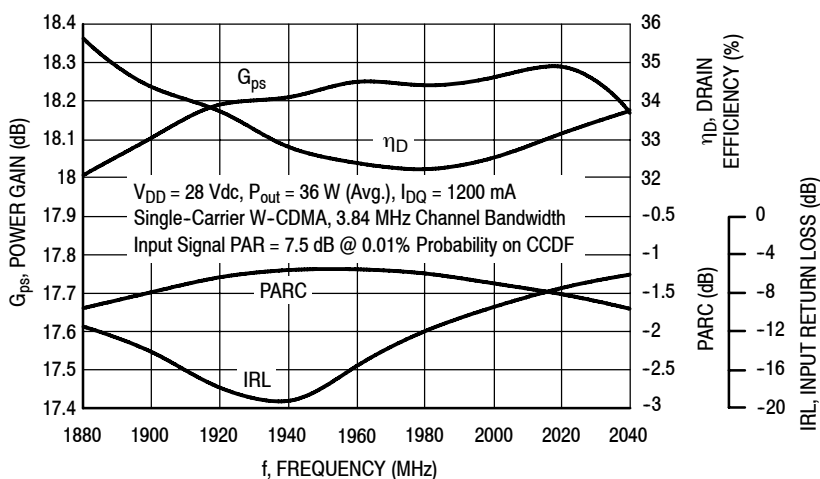
Figure 3. Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ P$_{out}$ = 36 Watts Avg.
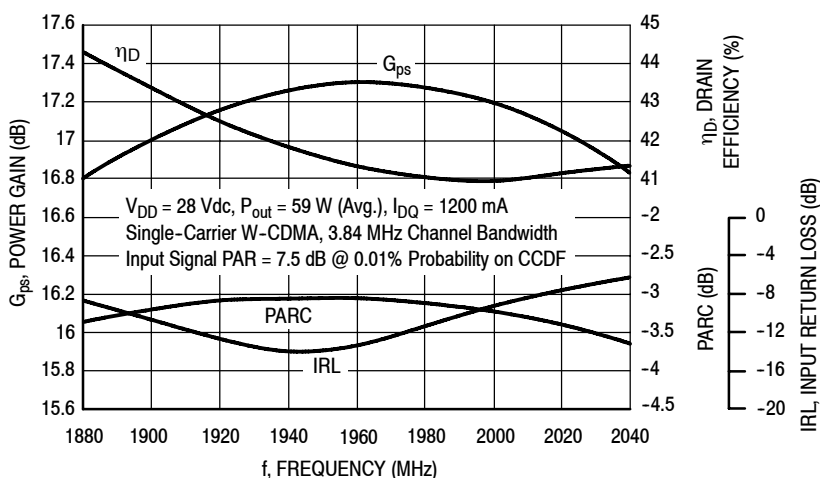
Figure 4. Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ P$_{out}$ = 59 Watts Avg.
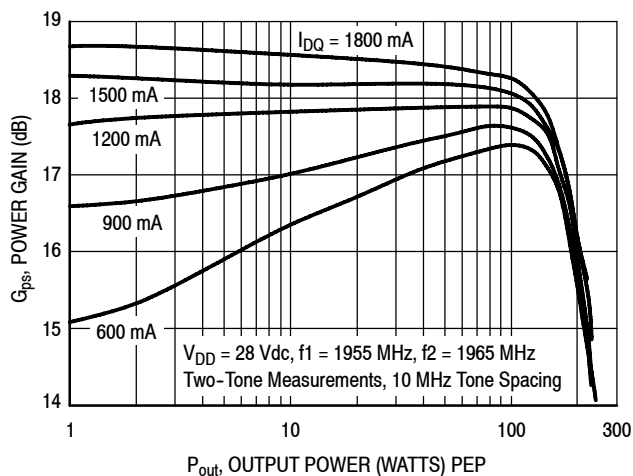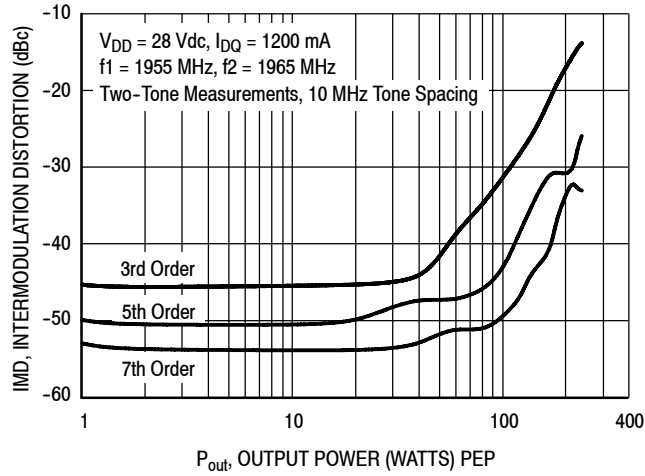

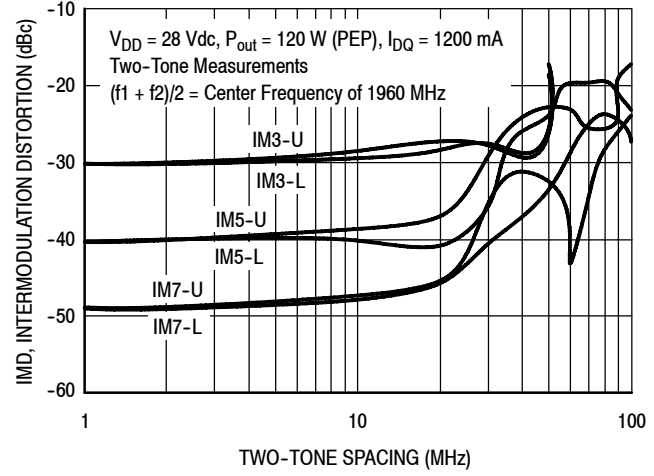**Figure 5. Two-Tone Power Gain versus Output Power**
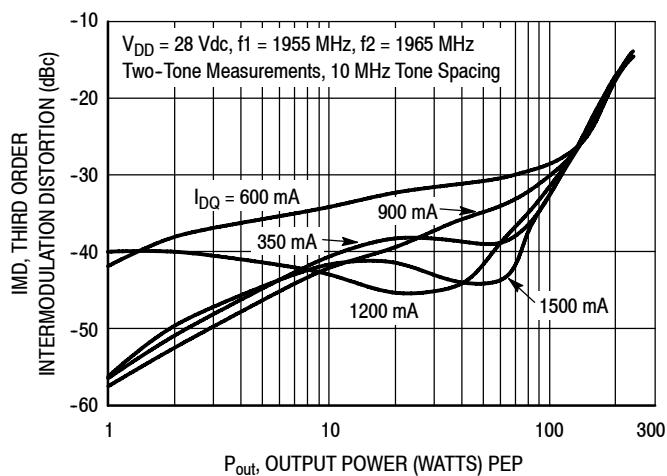
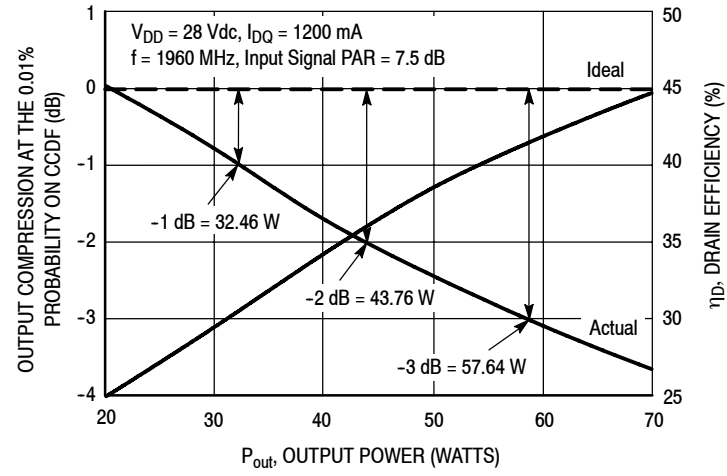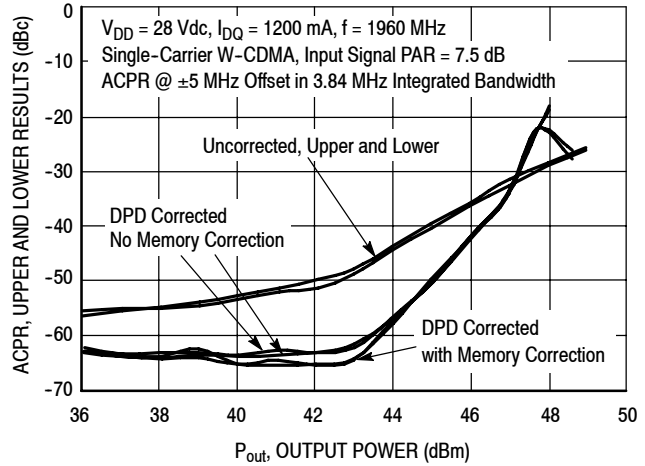**Figure 6. Third Order Intermodulation Distortion versus Output Power**

MRF7S19120NR1

TYPICAL CHARACTERISTICS

Figure 7. Intermodulation Distortion Products versus Output Power

Figure 8. Intermodulation Distortion Products versus Tone Spacing

Figure 9. Output Peak‑to‑Average Ratio Compression (PARC) versus Output Power

Figure 10. Digital Predistortion Correction versus ACPR and Output Power
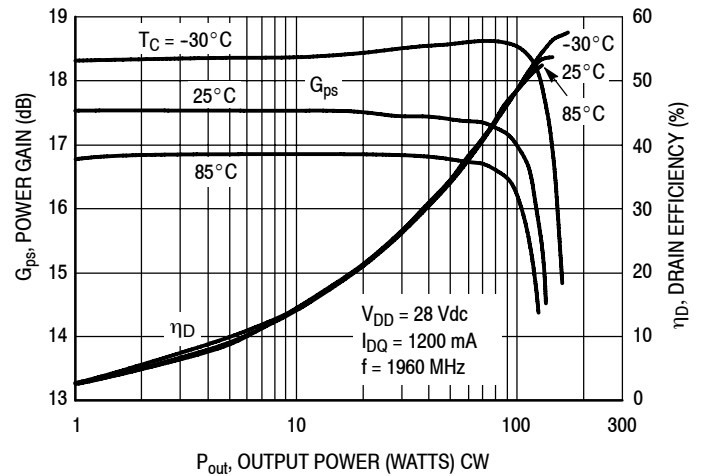
Figure 11. Power Gain and Drain Efficiency versus CW Output Power

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RF Device Data
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7

TYPICAL CHARACTERISTICS
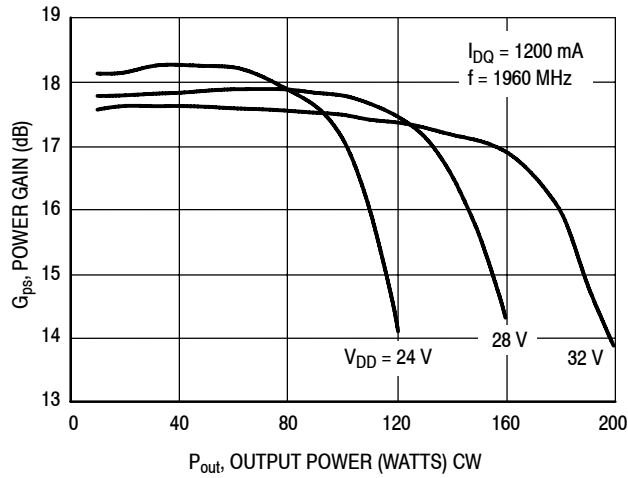
Figure 12. Power Gain versus Output Power

W-CDMA TEST SIGNAL
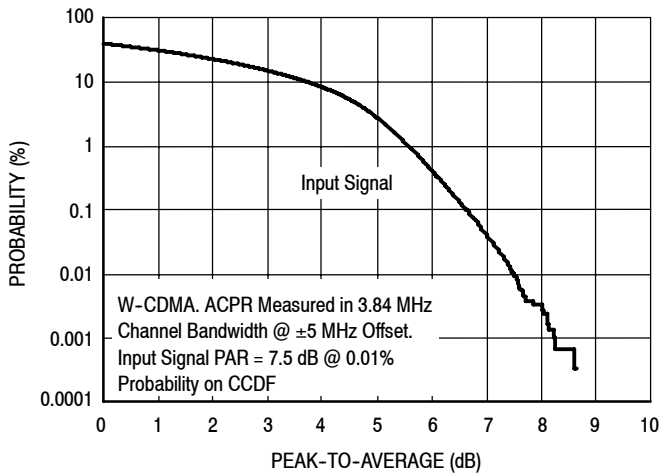
Figure 13. CCDF W–CDMA IQ Magnitude Clipping, Single-Carrier Test Signal
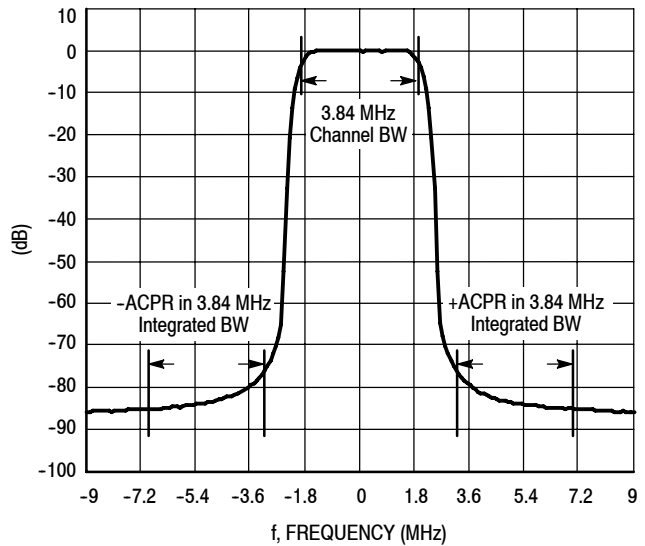
Figure 14. Single–Carrier W–CDMA Spectrum
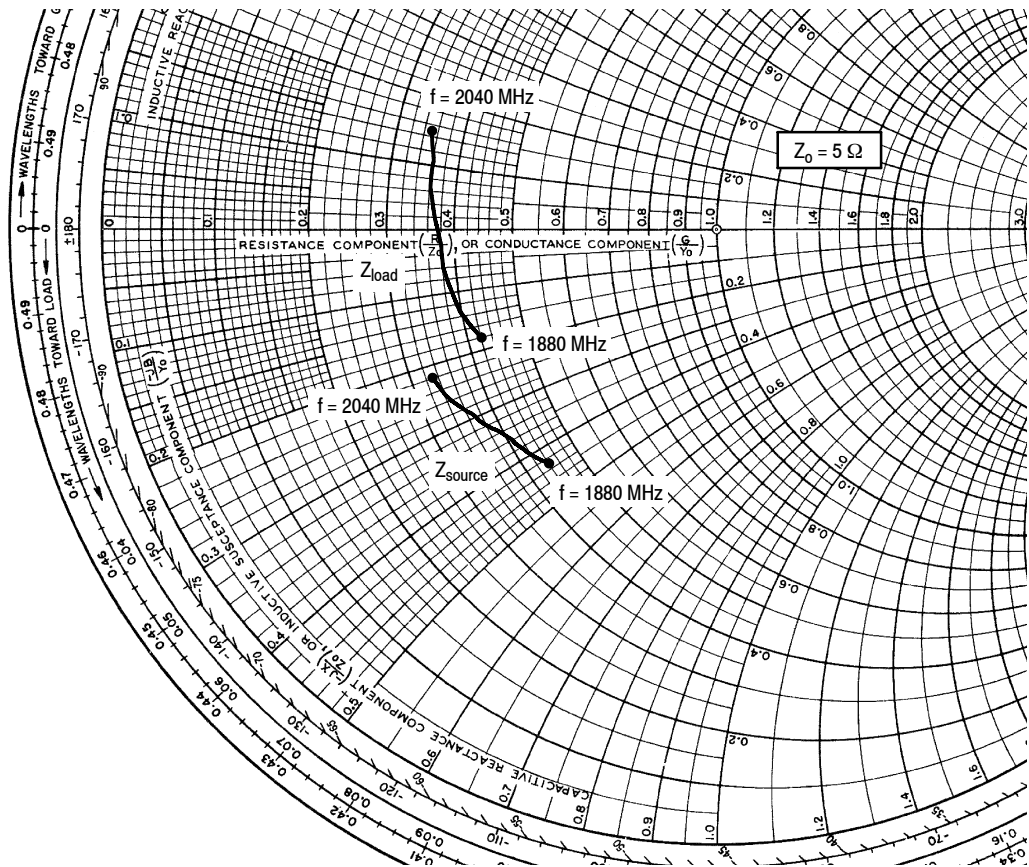
V_{DD} = 28 Vdc, I_{DQ} = 1200 mA, P_{out} = 36 W Avg.

f MHz	Z_source Ω	Z_load Ω
1880	2.195 – j2.157	2.091 – j0.905
1900	2.122 – j2.019	2.012 – j0.712
1920	2.054 – j1.880	1.957 – j0.515
1940	1.979 – j1.747	1.912 – j0.312
1960	1.922 – j1.623	1.887 – j0.089
1980	1.858 – j1.500	1.848 + j0.121
2000	1.793 – j1.380	1.819 + j0.327
2020	1.717 – j1.255	1.789 + j0.540
2040	1.645 – j1.112	1.761 + j0.756

Z_{source} = Test circuit impedance as measured from gate to ground.

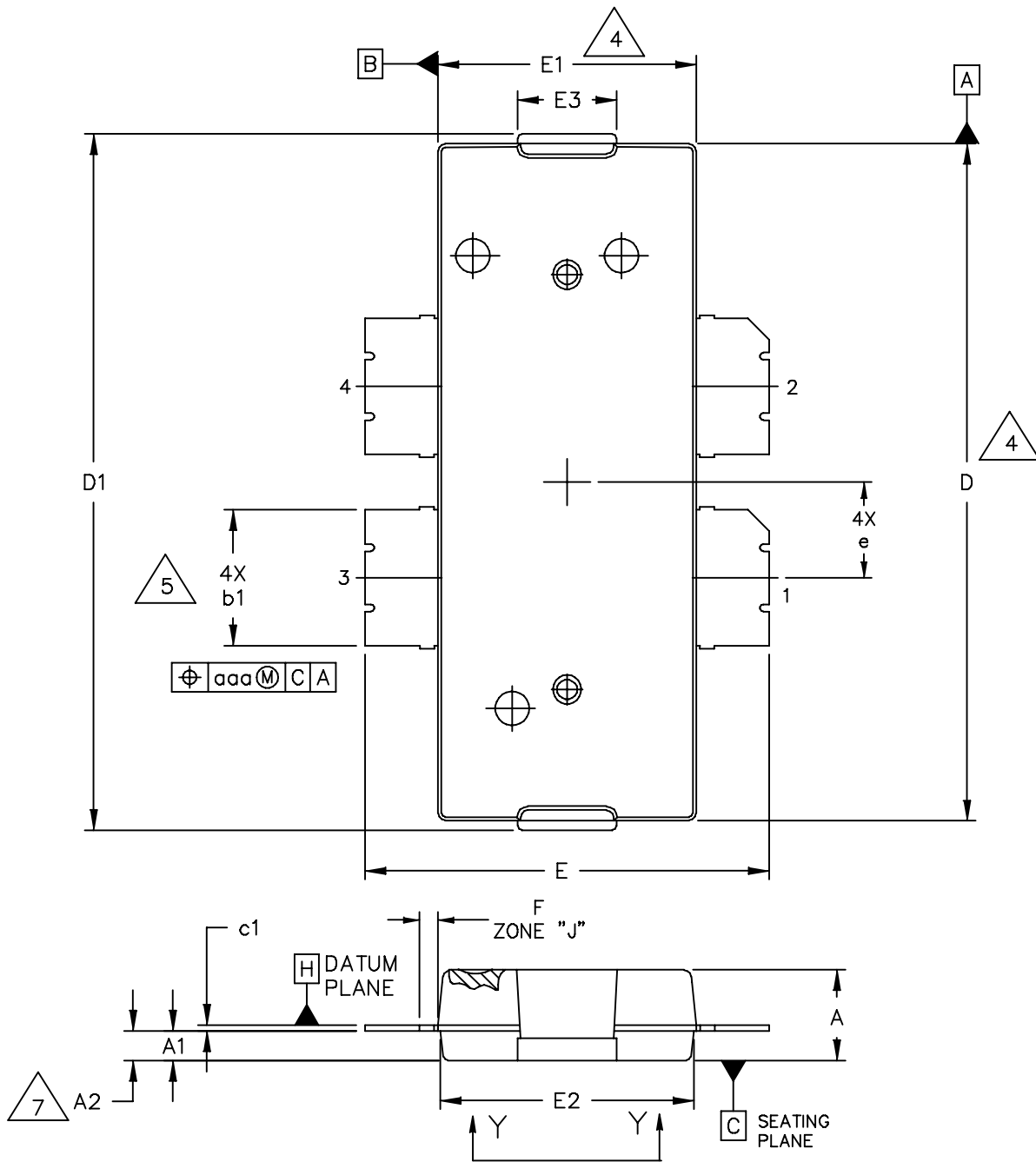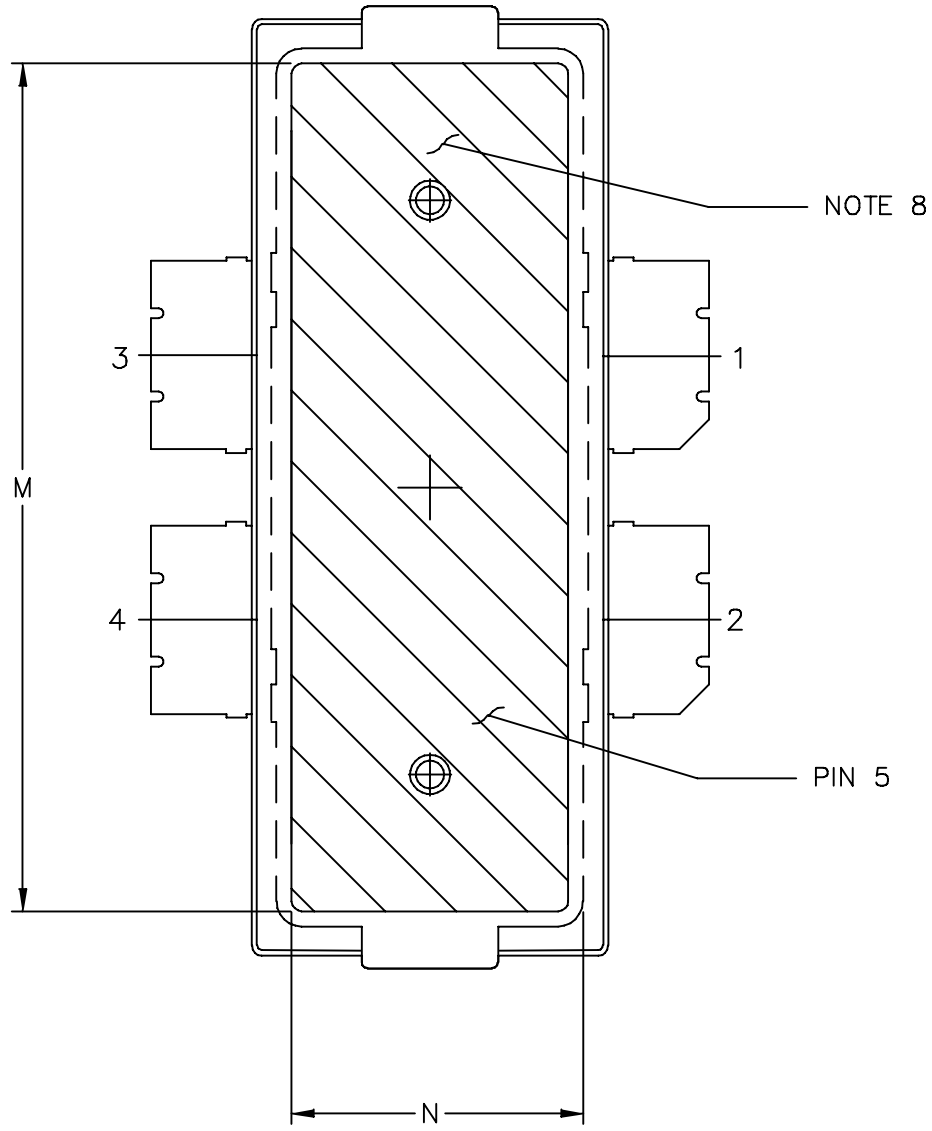Z_{load} = Test circuit impedance as measured from drain to ground.

Input Matching Network | Device Under Test | Output Matching Network

Z_{source} Z_{load}
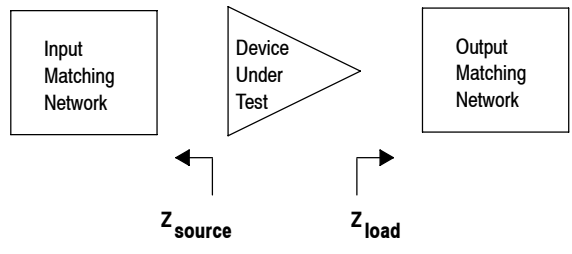
Figure 15. Series Equivalent Source and Load Impedance

PACKAGE DIMENSIONS

	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: TO−270 WIDEBODY LONG 4 LEAD (STRAIGHT LEAD)	DOCUMENT NO: 98ASA10882D	REV: A
	CASE NUMBER: 1730−02	30 JUL 2007
	STANDARD: NON−JEDEC	

VIEW Y–Y

MRF7S19120NR1

NOTES:

1. CONTROLLING DIMENSION: INCH

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M−1994.

3. DATUM PLANE −H− IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.

/4.\ DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 PER SIDE. THESE DIMENSIONS DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE −H−.

/5.\ DIMENSIONS DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 TOTAL IN EXCESS OF THIS DIMENSION AT MAXIMUM MATERIAL CONDITION.

6. DATUMS −A− AND −B− TO BE DETERMINED AT DATUM PLANE −H−.

/7.\ DIMENSION APPLIES WITHIN ZONE "J" ONLY.

8. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG.

PIN 1 − DRAIN   PIN 2 − DRAIN
PIN 3 − GATE   PIN 4 − GATEC
PIN 5 − SOURCE

DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX	DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX
A	.122	.128	3.12	3.23	b1	.184	.190	4.67	4.83
A1	.039	.043	0.99	1.09	c1	.007	.011	0.18	0.28
A2	.040	.042	1.02	1.07	e	.1315 BSC		3.34 BSC	
D	.928	.932	23.57	23.67	aaa	.004		0.10	
D1	.954	.958	24.23	24.33					
E	.551	.559	14	14.2					
E1	.353	.357	8.97	9.07					
E2	.346	.350	8.79	8.89					
E3	.132	.140	3.35	3.56					
F	.025 BSC		0.64 BSC						
M	.800	---	20.32	---					
N	.270	---	6.86	---					

MECHANICAL OUTLINE | PRINT VERSION NOT TO SCALE

TITLE:	DOCUMENT NO: 98ASA10882D	REV: A
TO−270 WIDEBODY LONG 4 LEAD (STRAIGHT LEAD)	CASE NUMBER: 1730−02	30 JUL 2007
	STANDARD: NON−JEDEC	

MRF7S19120NR1

PRODUCT DOCUMENTATION AND SOFTWARE

Refer to the following documents and software to aid your design process.

Application Notes

- AN1907: Solder Reflow Attach Method for High Power RF Devices in Plastic Packages
- AN1955: Thermal Measurement Methodology of RF Power Amplifiers
- AN3789: Clamping of High Power RF Transistors and RFICs in Over–Molded Plastic Packages

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

Software

- Electromigration MTTF Calculator

For Software, do a Part Number search at http://www.freescale.com, and select the "Part Number" link. Go to the Software & Tools tab on the part's Product Summary page to download the respective tool.

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Sept. 2007	• Initial Release of Data Sheet
1	Jan. 2009	• Updated Fig. 14, CCDF W–CDMA 3GPP, Test Model 1, 64 DPCH, 50% Clipping, Single–Carrier Test Signal, to better represent production test signal, p. 8 • Updated Fig. 16, Series Equivalent Source and Load Impedance, large signal Z_{source} impedance parameters to better reflect measured values, p. 9
2	Dec. 2009	• Updated Charge Device Model ESD from Class IV to III to reflect actual Qual Report results, p. 2 • Fig. 14, CCDF W–CDMA IQ Magnitude Clipping, Single–Carrier Test Signal and Fig. 15, Single–Carrier W–CDMA Spectrum updated to show the undistorted input test signal, p. 8 • Added AN1907, Solder Reflow Attach Method for High Power RF Devices in Plastic Packages and AN3789, Clamping of High Power RF Transistors and RFICs in Over–Molded Plastic Packages to Product Documentation, Application Notes, p. 13 • Added Electromigration MTTF Calculator availability to Product Software, p. 13
3	Mar. 2011	• Modified data sheet to reflect RF Test Reduction described in Product and Process Change Notification number, PCN13628, p. 1, 2 • Fig. 13, MTTF versus Junction Temperature removed, p. 8. Refer to the device's MTTF Calculator available at freescale.com/RFpower. Go to Design Resources > Software and Tools.

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