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3. Click the corresponding title from the search results.
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MB9A150RB Series

32-bit ARM® Cortex®-M3 FM3 Microcontroller

The MB9A150RB Series are highly integrated 32-bit microcontrollers dedicated for embedded controllers with low-power consumption mode and competitive cost.

These series are based on the ARM Cortex-M3 Processor with on-chip Flash memory and SRAM, and have peripheral functions such as various timers, ADCs, and Communication Interfaces (UART, CSIO, I²C).

The products which are described in this data sheet are placed into TYPE8 product categories in FM3 Family Peripheral Manual.

Features

32-bit ARM Cortex-M3 Core

- Processor version: r2p1
- Up to 40 MHz Frequency Operation
- Integrated Nested Vectored Interrupt Controller (NVIC): 1 NMI (non-maskable interrupt) and 48 peripheral interrupts and 16 priority levels
- 24-bit System timer (Sys Tick): System timer for OS task management

On-chip Memories

[Flash memory]

- Dual operation Flash memory
  - Dual Operation Flash memory has the upper bank and the lower bank.
    So, this series could implement erase, write and read operations
    for each bank simultaneously.
- Main area: Up to 512 Kbytes (Upto 496 Kbytes upper bank + 16 Kbytes lower bank)
- Work area: 32 Kbytes (lower bank)
- Read cycle: 0 wait-cycle
- Security function for code protection

[SRAM]

This Series on-chip SRAM is composed of two independent SRAM (SRAM0, SRAM1). SRAM0 is connected to I-code bus and D-code bus of Cortex-M3 core. SRAM1 is connected to System bus.

- SRAM0: Up to 32 Kbytes
- SRAM1: Up to 32 Kbytes

External Bus Interface

- Supports SRAM, NOR NAND Flash memory device
- Up to 8 chip selects
- 8-/16-bit Data width
- Up to 25-bit Address bit
- Maximum area size: Up to 256 Mbytes
- Supports Address/Data multiplex
- Supports external RDY function

Multi-function Serial Interface (Max 16 channels)

- 16 channels with 16 steps×9-bit FIFO
- Operation mode is selectable from the followings for each channel.
  - UART
  - CSIO
  - I²C

[UART]

- Full-duplex double buffer
- Selection with or without parity supported
- Built-in dedicated baud rate generator
- External clock available as a serial clock
- Hardware Flow control: Automatically control the transmission/reception by CTS/RTS (only ch.4)
- Various error detection functions available (parity errors, framing errors, and overrun errors)

[CSIO]

- Full-duplex double buffer
- Built-in dedicated baud rate generator
- Overrun error detection function available

[I²C]

Standard-mode (Max 100 kbps) / Fast-mode (Max 400 kbps) supported

DMA Controller (8channels)

The DMA Controller has an independent bus from the CPU, so CPU and DMA Controller can process simultaneously.

- 8 independently configured and operated channels
- Transfer can be started by software or request from the built-in peripherals
- Transfer address area: 32-bit (4 Gbytes)
- Transfer mode: Block transfer/Burst transfer/Demand transfer
- Transfer data type: byte/half-word/word
- Transfer block count: 1 to 16
- Number of transfers: 1 to 65536

A/D Converter (Max 24 channels) [12-bit A/D Converter]

- Successive Approximation type
- Built-in 2 units
- Conversion time: 2.0 µs @ 2.7 V to 3.6 V
- Priority conversion available (priority at 2 levels)
- Scanning conversion mode
- Built-in FIFO for conversion data storage (for SCAN conversion: 16 steps, for Priority conversion: 4 steps)

Base Timer (Max 16channels)

Operation mode is selectable from the followings for each channel.

- 16-bit PWM timer
- 16-bit PPG timer
- 16-/32-bit reload timer
- 16-/32-bit PWC timer

General-Purpose I/O Port

This series can use its pins as general-purpose I/O ports when they are not used for external bus or peripherals. Moreover, the port relocate function is built in. It can set which I/O port the peripheral function can be allocated to.

- Capable of pull-up control per pin
- Capable of reading pin level directly
- Built-in the port relocate function
- Up to 103 high-speed general-purpose I/O Ports@120 pin Package
- Some ports are 5 V tolerant I/O

See List of Pin Function and I/O Circuit Type to confirm the corresponding pins.

Dual Timer (32-/16-bit Down Counter)

The Dual Timer consists of two programmable 32-/16-bit down counters.

Operation mode is selectable from the followings for each channel.

- Free-running
- Periodic (=Reload)
- One-shot

Multi-function Timer

The Multi-function timer is composed of the following blocks.

- 16-bit free-run timer × 3ch.
- Input capture × 4ch.
- Output compare × 6ch.
- A/D activation compare × 2ch.
- Waveform generator × 3ch.
- 16-bit PPG timer × 3ch.

The following function can be used to achieve the motor control.

- PWM signal output function
- DC chopper waveform output function
- Dead time function
- Input capture function
- A/D convertor activate function
- DTIF (Motor emergency stop) interrupt function

Quadrature Position/Revolution Counter (QPRC)

The Quadrature Position/Revolution Counter (QPRC) is used to measure the position of the position encoder. Moreover, it is possible to use as the up/down counter.

- The detection edge of the three external event input pins AIN, BIN and ZIN is configurable.
- 16-bit position counter
- 16-bit revolution counter
- Two 16-bit compare registers

HDMI-CEC/Remote Control Reception (Up to 2 channels)

HDMI-CEC transmission

- Header block automatic transmission by judging Signal free
- Generating status interrupt by detecting Arbitration lost
- Generating START, EOM, ACK automatically to output CEC transmission by setting 1 byte data
- Generating transmission status interrupt when transmitting 1 block (1 byte data and EOM/ACK)

HDMI-CEC reception

- Automatic ACK reply function available
- Line error detection function available

Remote control reception

- 4 bytes reception buffer
- Repeat code detection function available

Real-time clock (RTC)

The Real-time clock can count Year/Month/Day/Hour/Minute/Second/A day of the week from 00 to 99.

- The interrupt function with specifying date and time (Year/Month/Day/Hour/Minute) is available. This function is also available by specifying only Year, Month, Day, Hour or Minute.
- Timer interrupt function after set time or each set time.
- Capable of rewriting the time with continuing the time count.
- Leap year automatic count is available.

Watch Counter
The Watch counter is used for wake up from sleep and timer mode.

Interval timer: up to 64 s (Max) @ Sub Clock : 32.768 kHz

External Interrupt Controller Unit
- Up to 24 external interrupt input pins
- Include one non-maskable interrupt (NMI) input pin

Watchdog Timer (Two channels)
A watchdog timer can generate interrupts or a reset when a time-out value is reached.

This series consists of two different watchdogs, a "Hardware" watchdog and a "Software" watchdog.

The Hardware watchdog timer is clocked by the built-in Low-speed CR oscillator. Therefore, the Hardware watchdog is active in any low-power consumption modes except RTC, Stop, Deep Standby RTC and Deep Standby Stop modes.

CRC (Cyclic Redundancy Check) Accelerator
The CRC accelerator calculates the CRC which has a heavy software processing load, and achieves a reduction of the integrity check processing load for reception data and storage.

CCITT CRC16 and IEEE-802.3 CRC32 are supported.

- CCITT CRC16 Generator Polynomial: 0x1021
- IEEE-802.3 CRC32 Generator Polynomial: 0x04C11DB7

Clock and Reset

[Clocks]

Selectable from five clock sources (2 external oscillators, 2 built-in CR oscillators, and Main PLL).

- Main Clock: 4 MHz to 48 MHz
- Sub Clock: 32.768 kHz
- Built-in High-speed CR Clock: 4 MHz
- Built-in Low-speed CR Clock: 100 kHz
- Main PLL Clock

[Resets]

- Reset requests from INITX pin
- Power-on reset
- Software reset
- Watchdog timers reset
- Low-voltage detection reset
- Clock Super Visor reset

Clock Super Visor (CSV)
Clocks generated by built-in CR oscillators are used to supervise abnormality of the external clocks.

- If external clock failure (clock stop) is detected, reset is asserted.
- If external frequency anomaly is detected, interrupt or reset is asserted.

Low-Voltage Detector (LVD)
This Series includes 2-stage monitoring of voltage on the VCC pins. When the voltage falls below the voltage that has been set, Low-Voltage Detector generates an interrupt or reset.

- LVD1: error reporting via interrupt
- LVD2: auto-reset operation

Low-Power Consumption Mode
Six low-power consumption modes supported.

- Sleep
- Timer
- RTC
- Stop
- Deep Standby RTC (selectable between keeping the value of RAM and not)
- Deep Standby Stop (selectable between keeping the value of RAM and not)

Debug
- Serial Wire JTAG Debug Port (SWJ-DP)
- Embedded Trace Macrocells (ETM).*

*: MB9AF154MB, F155MB and F156MB support only SWJ-DP.

Unique ID
Unique value of the device (41-bit) is set.

Power Supply
Wide range voltage: VCC = 1.65 V to 3.6 V

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1. Product Lineup

1.1 Memory size

Product name		MB9AF154MB/NB/RB	MB9AF155MB/NB/RB	MB9AF156MB/NB/RB
On-chip Flash memory	Main area	256 Kbytes	384 Kbytes	512 Kbytes
	Work area	32 Kbytes	32 Kbytes	32 Kbytes
On-chip SRAM	SRAM0	16 Kbytes	24 Kbytes	32 Kbytes
	SRAM1	16 Kbytes	24 Kbytes	32 Kbytes
	Total	32 Kbytes	48 Kbytes	64 Kbytes

1.2 Function

Product name			MB9AF154MB MB9AF155MB MB9AF156MB	MB9AF154NB MB9AF155NB MB9AF156NB	MB9AF154RB MB9AF155RB MB9AF156RB
Pin count			80/96	100/112	120
CPU			Cortex-M3		
	Freq.		40 MHz		
Power supply voltage range			1.65V to 3.6V		
DMAC			8ch.		
External Bus Interface			Addr: 21-bit (Max) R/W Data: 8-bit (Max) CS: 4 (Max) Support: SRAM, NOR Flash memory	Addr: 25-bit (Max) R/W Data: 8-/16-bit (Max) CS: 8 (Max) Support: SRAM, NOR Flash memory	Addr: 25-bit (Max) R/W Data: 8-/16-bit (Max) CS: 8 (Max) Support: SRAM, NOR Flash memory, NAND Flash memory
Multi-function Serial Interface (UART/CSIO/I^{2}C)			10ch. (Max) Enabled channels : ch.0 to ch.7, ch.10, ch.11	14ch. (Max) Enabled channels : ch.0 to ch.13	16ch. (Max) Enabled channels : ch.0 to ch.15
Base Timer (PWC/Reload timer/PWM/PPG)			16ch. (Max)		
MF-Timer	A/D activation compare	2ch.	1 unit (Max)		
	Input capture	4ch.			
	Free-run timer	3ch.			
	Output compare	6ch.			
	Waveform generator	3ch.			
	PPG	3ch.			
QPRC			2ch. (Max)		
Dual Timer			1 unit		
HDMI-CEC/ Remote Control Reception			2ch. (Max)		

Product name		MB9AF154MB MB9AF155MB MB9AF156MB	MB9AF154NB MB9AF155NB MB9AF156NB	MB9AF154RB MB9AF155RB MB9AF156RB
Real-Time Clock		1 unit		
Watch Counter		1 unit		
CRC Accelerator		Yes		
Watchdog timer		1ch. (SW) + 1ch. (HW)		
External Interrupts		23 pins (Max) + NMI × 1	24 pins (Max) + NMI × 1	
I/O ports		66 pins (Max)	83 pins (Max)	103 pins (Max)
12-bit A/D converter		17ch. (2 units)	24ch. (2 units)	
CSV (Clock Super Visor)		Yes		
LVD (Low-Voltage Detector)		2ch.		
Built-in CR	High-speed	4 MHz		
	Low-speed	100 kHz		
Debug Function		SWJ-DP	SWJ-DP/ETM	
Unique ID		Yes		

Note:

- *All signals of the peripheral function in each product cannot be allocated by limiting the pins of package. It is necessary to use the port relocate function of the I/O port according to your function use.*
- *See Electrical Characteristics0 AC Characteristics 12.4.3 Built-in CR Oscillation Characteristics for accuracy of built-in CR.*

2. Packages

Package \ Product name	MB9AF154MB MB9AF155MB MB9AF156MB	MB9AF154NB MB9AF155NB MB9AF156NB	MB9AF154RB MB9AF155RB MB9AF156RB
LQFP: LQH080 (0.5 mm pitch)	❍	-	-
BGA: FDG096 (0.5 mm pitch)	❍	-	-
LQFP: LQI100 (0.5 mm pitch)	-	❍	-
BGA: LBC112 (0.8 mm pitch)	-	❍	-
LQFP: LQM120 (0.5 mm pitch)	-	-	❍

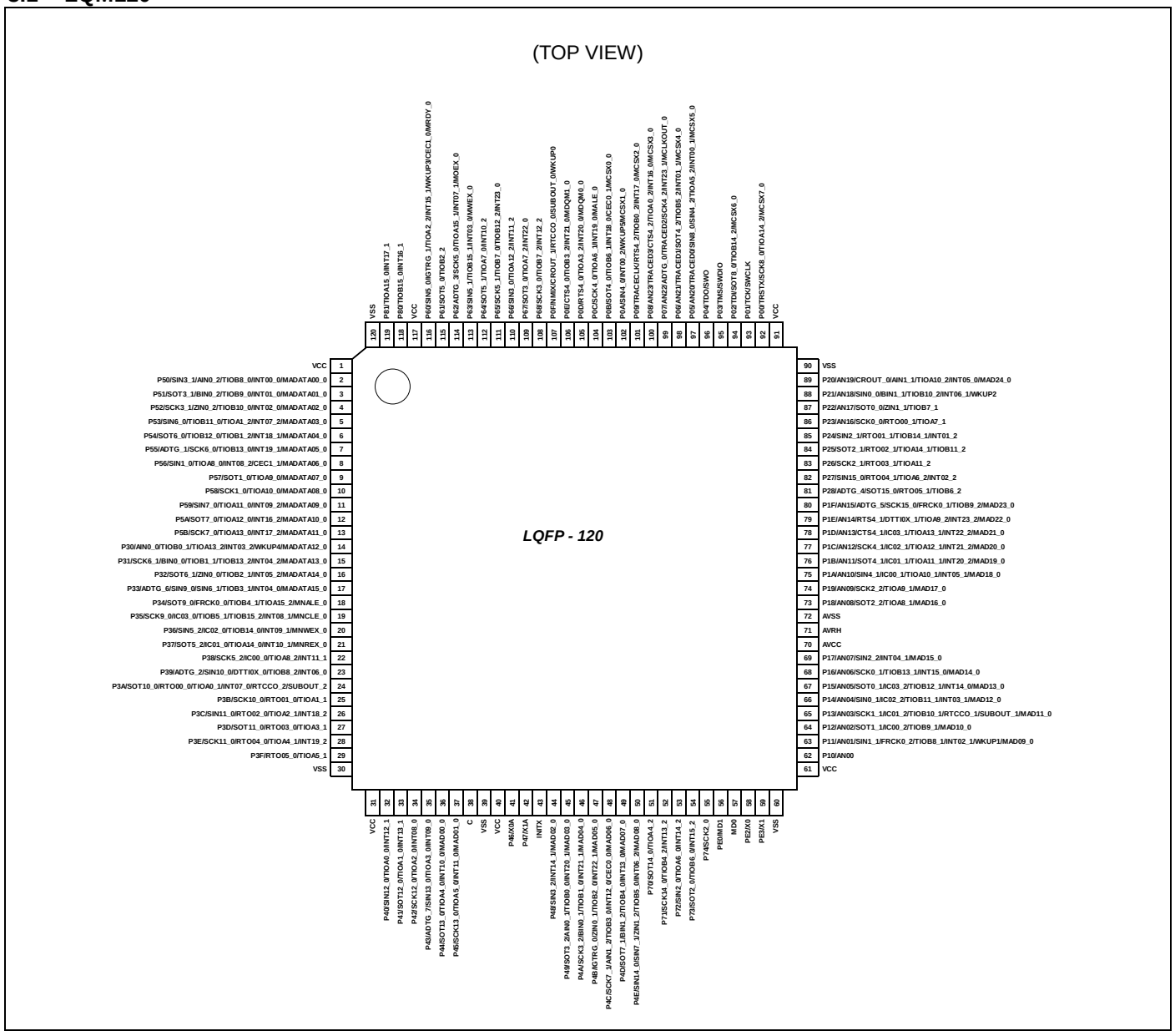
❍: Supported

Note:

- *See Package Dimensions for detailed information on each package.*

3. Pin Assignment

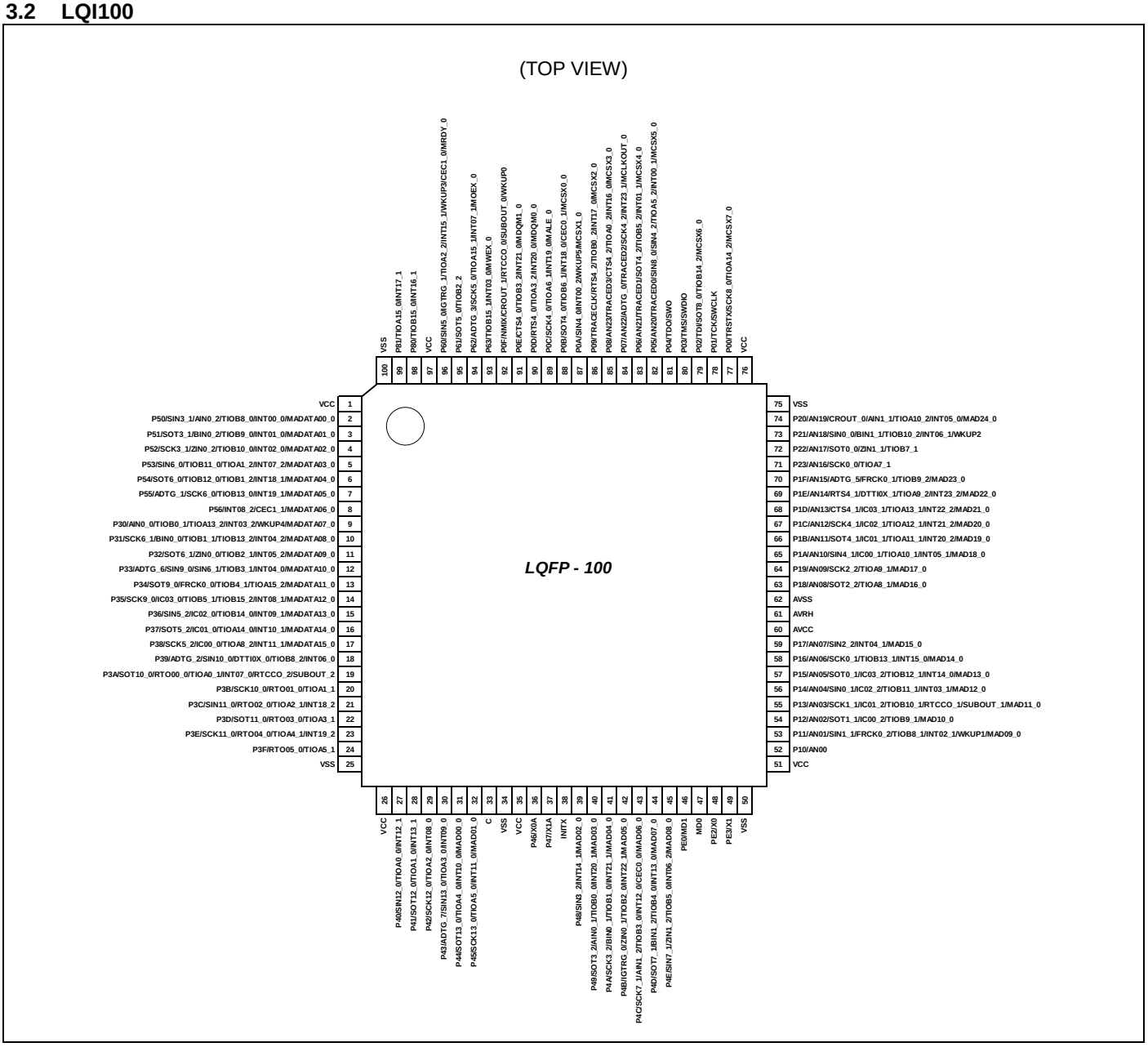
3.1 LQM120



Note:

- *The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.*

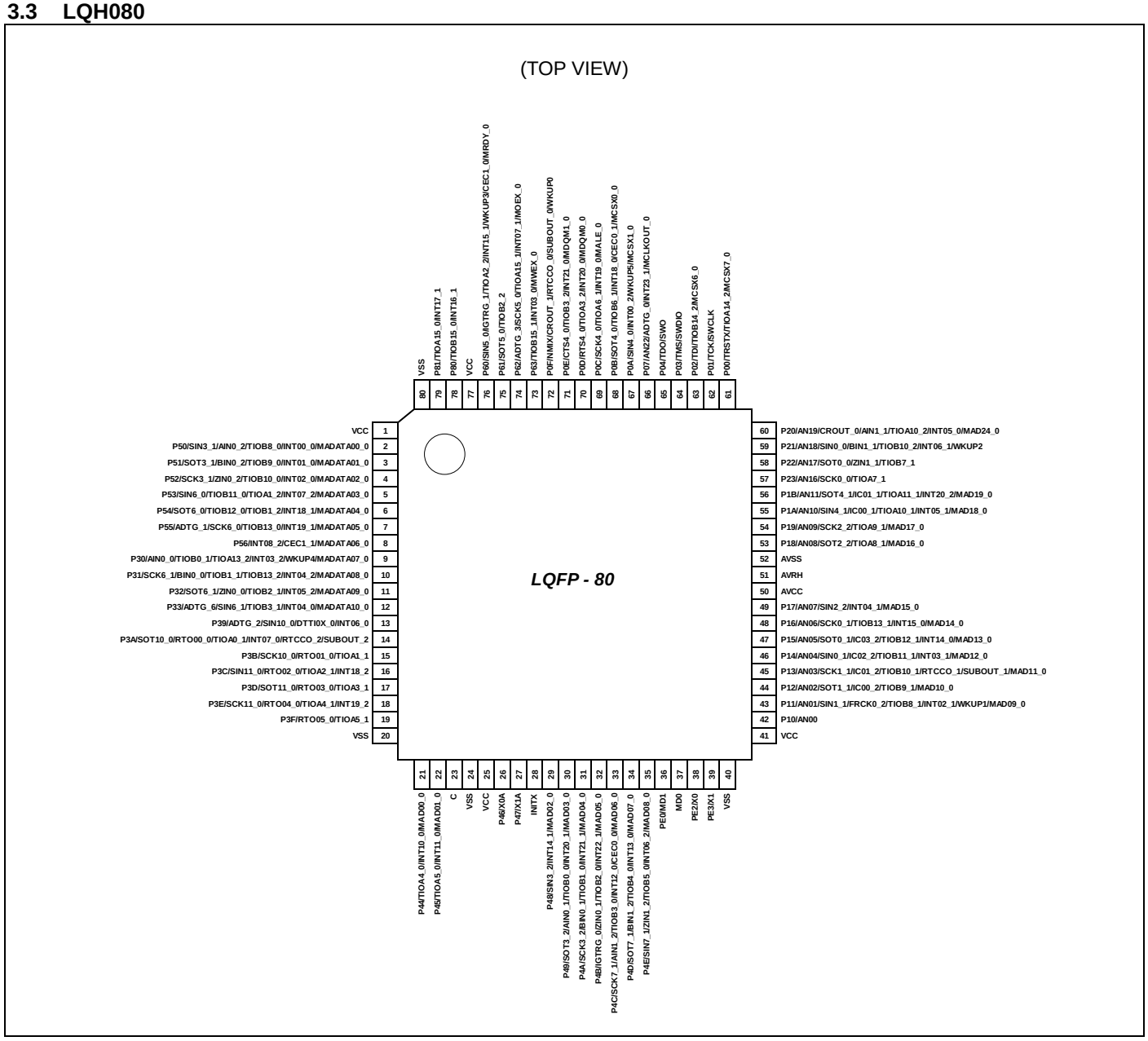
3.2 LQI100



Note:

- *The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.*

3.3 LQH080



Note:

- *The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.*

3.4 LBC112

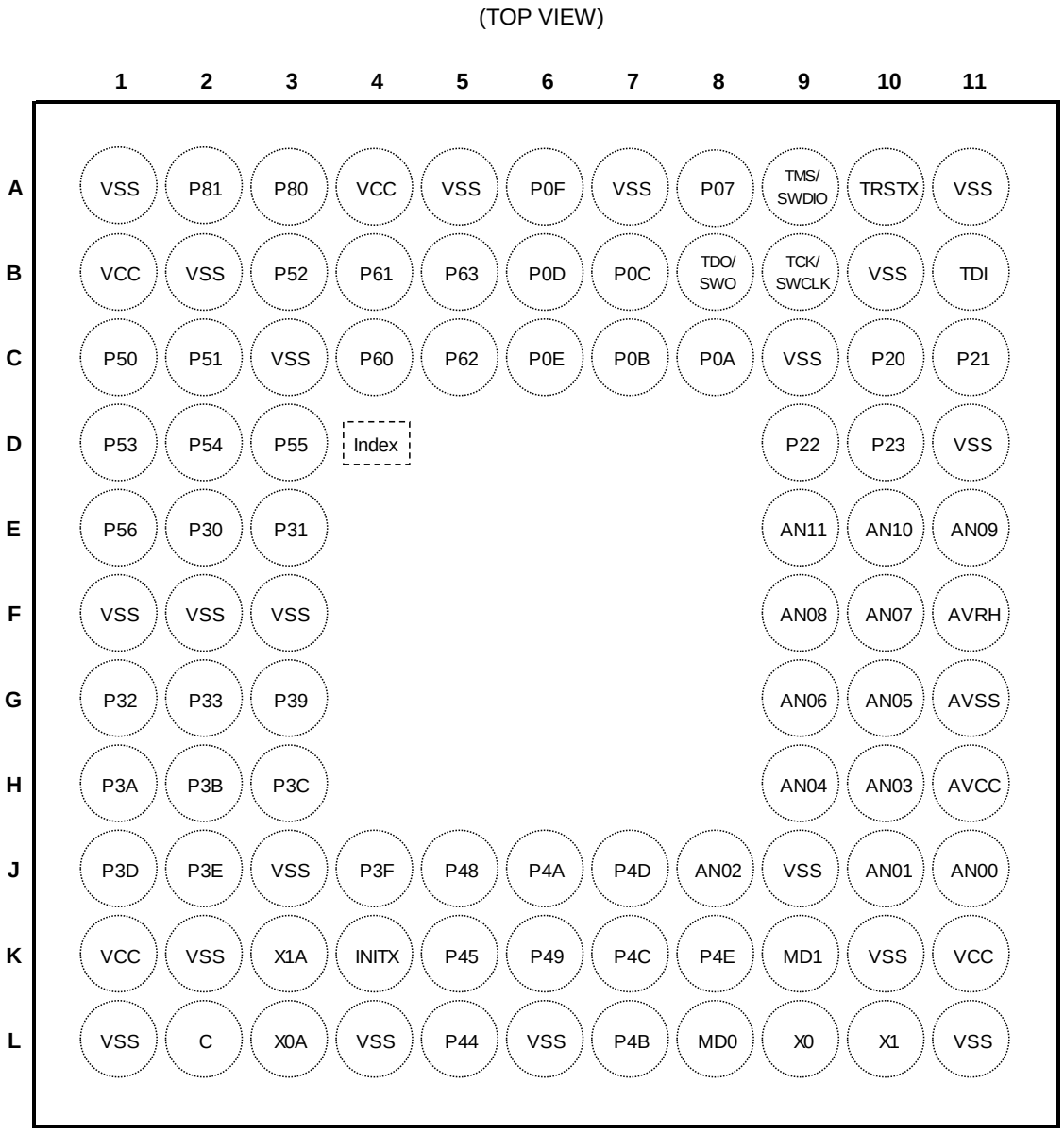
(TOP VIEW)

	1	2	3	4	5	6	7	8	9	10	11
A	VSS	P81	P80	VCC	P0E	P0B	P07	TMS/ SWDIO	TRSTX	VCC	VSS
B	VCC	VSS	P52	P61	P0F	P0C	P08	TDO/ SWO	TCK/ SWCLK	VSS	TDI
C	P50	P51	VSS	P60	P62	P0D	P09	P05	VSS	P20	P21
D	P53	P54	P55	VSS	P56	P63	P0A	VSS	P06	P23	AN15
E	P30	P31	P32	P33	Index			P22	AN14	AN12	AN11
F	P34	P35	P36	P39				AN13	AN10	AN09	AVRH
G	P37	P38	P3A	P3D				AN08	AN07	AN06	AVSS
H	P3B	P3C	P3E	VSS	P44	P4C	AN05	VSS	AN04	AN03	AVCC
J	VCC	P3F	VSS	P40	P43	P49	P4D	AN02	VSS	AN01	AN00
K	VCC	VSS	X1A	INITX	P42	P48	P4B	P4E	MD1	VSS	VCC
L	VSS	C	X0A	VSS	P41	P45	P4A	MD0	X0	X1	VSS

Note:

- *The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.*

3.5 FDG096



Note:

- *The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.*

4. List of Pin Function

4.1 List of Pin Numbers

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

Pin No					Pin Name	I/O Circuit Type	Pin State Type
LQFP-120	LQFP-100	BGA-112	LQFP-80	BGA-96			
1	1	B1	1	B1	VCC	-	
2	2	C1	2	C1	P50	E	K
					SIN3_1		
					AIN0_2		
					TIOB8_0		
					INT00_0		
					MADATA00_0		
3	3	C2	3	C2	P51	E	K
					SOT3_1 (SDA3_1)		
					BIN0_2		
					TIOB9_0		
					INT01_0		
					MADATA01_0		
4	4	B3	4	B3	P52	E	K
					SCK3_1 (SCL3_1)		
					ZIN0_2		
					TIOB10_0		
					INT02_0		
					MADATA02_0		
5	5	D1	5	D1	P53	E	K
					SIN6_0		
					TIOB11_0		
					TIOA1_2		
					INT07_2		
					MADATA03_0		

Pin No					Pin Name	I/O Circuit Type	Pin State Type
LQFP-120	LQFP-100	BGA-112	LQFP-80	BGA-96			
6	6	D2	6	D2	P54	E	K
					SOT6_0 (SDA6_0)		
					TIOB12_0		
					TIOB1_2		
					INT18_1		
					MADATA04_0		
7	7	D3	7	D3	P55	E	K
					ADTG_1		
					SCK6_0 (SCL6_0)		
					TIOB13_0		
					INT19_1		
					MADATA05_0		
8	8	D5	8	E1	P56	H[1]	R
					INT08_2		
					CEC1_1		
					MADATA06_0		
	-	-	-	-	SIN1_0		
					TIOA8_0		
9	-	-	-	-	P57	H[1]	J
					SOT1_0 (SDA1_0)		
					TIOA9_0		
					MADATA07_0		
10	-	-	-	-	P58	H[1]	J
					SCK1_0 (SCL1_0)		
					TIOA10_0		
					MADATA08_0		

Pin No					Pin Name	I/O Circuit Type	Pin State Type
LQFP-120	LQFP-100	BGA-112	LQFP-80	BGA-96			
11	-	-	-	-	P59 SIN7_0 TIOA11_0 INT09_2 MADATA09_0	E	K
12	-	-	-	-	P5A SOT7_0 (SDA7_0) TIOA12_0 INT16_2 MADATA10_0	E	K
13	-	-	-	-	P5B SCK7_0 (SCL7_0) TIOA13_0 INT17_2 MADATA11_0	E	K
14	-	-	-	-	P30 AIN0_0 TIOB0_1 TIOA13_2 INT03_2 WKUP4 MADATA12_0	E	S
-	9	E1	9	E2	P30 AIN0_0 TIOB0_1 TIOA13_2 INT03_2 WKUP4 MADATA07_0	E	S

Pin No					Pin Name	I/O Circuit Type	Pin State Type
LQFP-120	LQFP-100	BGA-112	LQFP-80	BGA-96			
15	-	-	-	-	P31 SCK6_1 (SCL6_1) BIN0_0 TIOB1_1 TIOB13_2 INT04_2 MADATA13_0	E	K
-	10	E2	10	E3	P31 SCK6_1 (SCL6_1) BIN0_0 TIOB1_1 TIOB13_2 INT04_2 MADATA08_0	E	K
16	-	-	-	-	P32 SOT6_1 (SDA6_1) ZIN0_0 TIOB2_1 INT05_2 MADATA14_0	E	K
-	11	E3	11	G1	P32 SOT6_1 (SDA6_1) ZIN0_0 TIOB2_1 INT05_2 MADATA09_0	E	K
17	-	-	-	-	P33 ADTG_6 SIN9_0 SIN6_1 TIOB3_1 INT04_0 MADATA15_0	E	K

Pin No					Pin Name	I/O Circuit Type	Pin State Type
LQFP-120	LQFP-100	BGA-112	LQFP-80	BGA-96			
-	12	E4	12	G2	P33	E	K
					ADTG_6		
					SIN6_1		
					TIOB3_1		
					INT04_0		
					MADATA10_0		
			-	-	SIN9_0		
18	-	-	-	-	P34	E	J
					SOT9_0 (SDA9_0)		
					FRCK0_0		
					TIOB4_1		
					TIOA15_2		
					MNALE_0		
-	13	F1	-	-	P34	E	J
					SOT9_0 (SDA9_0)		
					FRCK0_0		
					TIOB4_1		
					TIOA15_2		
					MADATA11_0		
19	-	-	-	-	P35	E	K
					SCK9_0 (SCL9_0)		
					IC03_0		
					TIOB5_1		
					TIOB15_2		
					INT08_1		
					MNCLE_0		
-	14	F2	-	-	P35	E	K
					SCK9_0 (SCL9_0)		
					IC03_0		
					TIOB5_1		
					TIOB15_2		
					INT08_1		
					MADATA12_0		

Pin No					Pin Name	I/O Circuit Type	Pin State Type
LQFP-120	LQFP-100	BGA-112	LQFP-80	BGA-96			
20	-	-	-	-	P36	E	K
					SIN5_2		
					IC02_0		
					TIOB14_0		
					INT09_1		
					MNWEX_0		
-	15	F3	-	-	P36	E	K
					SIN5_2		
					IC02_0		
					TIOB14_0		
					INT09_1		
					MADATA13_0		
-	-	-	-	F1	VSS	-	
-	-	-	-	F2	VSS	-	
-	-	-	-	F3	VSS	-	
21	-	-	-	-	P37	E	K
					SOT5_2 (SDA5_2)		
					IC01_0		
					TIOA14_0		
					INT10_1		
					MNREX_0		
-	16	G1	-	-	P37	E	K
					SOT5_2 (SDA5_2)		
					IC01_0		
					TIOA14_0		
					INT10_1		
					MADATA14_0		

Pin No					Pin Name	I/O Circuit Type	Pin State Type
LQFP-120	LQFP-100	BGA-112	LQFP-80	BGA-96			
22	17	G2	-	-	P38	E	K
					SCK5_2 (SCL5_2)		
					IC00_0		
					TIOA08_2		
					INT11_1		
-					MADATA15_0		
23	18	F4	13	G3	P39	E	K
					ADTG_2		
					SIN10_0		
					DTTI0X_0		
					INT06_0		
			-	-	TIOB8_2		
24	19	G3	14	H1	P3A	E	K
					SOT10_0 (SDA10_0)		
					RTO00_0		
					TIOA0_1		
					INT07_0		
					RTCCO_2		
					SUBOUT_2		
25	20	H1	15	H2	P3B	E	J
					SCK10_0 (SCL10_0)		
					RTO01_0		
					TIOA1_1		
26	21	H2	16	H3	P3C	E	K
					SIN11_0		
					RTO02_0		
					TIOA2_1		
					INT18_2		

Pin No					Pin Name	I/O Circuit Type	Pin State Type
LQFP-120	LQFP-100	BGA-112	LQFP-80	BGA-96			
27	22	G4	17	J1	P3D SOT11_0 (SDA11_0) RTO03_0 TIOA3_1	E	J
-	-	B2	-	B2	VSS	-	
28	23	H3	18	J2	P3E SCK11_0 (SCL11_0) RTO04_0 TIOA4_1 INT19_2	E	K
29	24	J2	19	J4	P3F RTO05_0 TIOA5_1	E	J
30	25	L1	20	L1	VSS	-	
31	26	J1	-	-	VCC	-	
32	27	J4	-	-	P40 SIN12_0 TIOA0_0 INT12_1	E	K
33	28	L5	-	-	P41 SOT12_0 (SDA12_0) TIOA1_0 INT13_1	E	K
34	29	K5	-	-	P42 SCK12_0 (SCL12_0) TIOA2_0 INT08_0	E	K

Pin No					Pin Name	I/O Circuit Type	Pin State Type
LQFP-120	LQFP-100	BGA-112	LQFP-80	BGA-96			
35	30	J5	-	-	P43	E	K
					ADTG_7		
					SIN13_0		
					TIOA3_0		
					INT09_0		
36	31	H5	21	L5	P44	E	K
			-	-	SOT13_0 (SDA13_0)		
			21	L5	TIOA4_0		
					INT10_0		
					MAD00_0		
37	32	L6	22	K5	P45	E	K
			-	-	SCK13_0		
			22	K5	TIOA5_0		
					INT11_0		
					MAD01_0		
-	-	K2	-	K2	VSS	-	
-	-	J3	-	J3	VSS	-	
-	-	H4	-	-	VSS	-	
-	-	-	-	L6	VSS	-	
38	33	L2	23	L2	C	-	
39	34	L4	24	L4	VSS	-	
40	35	K1	25	K1	VCC	-	
41	36	L3	26	L3	P46	D	F
					X0A		
42	37	K3	27	K3	P47	D	G
					X1A		
43	38	K4	28	K4	INITX	B	C
44	39	K6	29	J5	P48	E	K
					SIN3_2		
					INT14_1		
					MAD02_0		

Pin No					Pin Name	I/O Circuit Type	Pin State Type
LQFP-120	LQFP-100	BGA-112	LQFP-80	BGA-96			
45	40	J6	30	K6	P49	E	K
					SOT3_2 (SDA3_2)		
					AIN0_1		
					TIOB0_0		
					INT20_1		
					MAD03_0		
46	41	L7	31	J6	P4A	E	K
					SCK3_2 (SCL3_2)		
					BIN0_1		
					TIOB1_0		
					INT21_1		
					MAD04_0		
47	42	K7	32	L7	P4B	E	K
					IGTRG_0		
					ZIN0_1		
					TIOB2_0		
					INT22_1		
					MAD05_0		
48	43	H6	33	K7	P4C	H[1]	R
					SCK7_1 (SCL7_1)		
					AIN1_2		
					TIOB3_0		
					INT12_0		
					CEC0_0		
					MAD06_0		

Pin No					Pin Name	I/O Circuit Type	Pin State Type
LQFP-120	LQFP-100	BGA-112	LQFP-80	BGA-96			
49	44	J7	34	J7	P4D	H[1]	K
					SOT7_1 (SDA7_1)		
					BIN1_2		
					TIOB4_0		
					INT13_0		
					MAD07_0		
50	45	K8	35	K8	P4E	H[1]	K
					SIN7_1		
					ZIN1_2		
					TIOB5_0		
					INT06_2		
					MAD08_0		
	-	-	-	-	SIN14_0		
51	-	-	-	-	P70	E	J
					SOT14_0 (SDA14_0)		
					TIOA4_2		
52	-	-	-	-	P71	E	K
					SCK14_0 (SCL14_0)		
					TIOB4_2		
					INT13_2		
53	-	-	-	-	P72	E	K
					SIN2_0		
					TIOA6_0		
					INT14_2		
54	-	-	-	-	P73	E	K
					SOT2_0 (SDA2_0)		
					TIOB6_0		
					INT15_2		

Pin No					Pin Name	I/O Circuit Type	Pin State Type
LQFP-120	LQFP-100	BGA-112	LQFP-80	BGA-96			
55	-	-	-	-	P74	E	J
					SCK2_0 (SCL2_0)		
56	46	K9	36	K9	MD1	C	E
					PE0		
57	47	L8	37	L8	MD0	G	D
58	48	L9	38	L9	X0	A	A
					PE2		
59	49	L10	39	L10	X1	A	B
					PE3		
60	50	L11	40	L11	VSS	-	
61	51	K11	41	K11	VCC	-	
62	52	J11	42	J11	P10	F	L
					AN00		
63	53	J10	43	J10	P11	F	P
					AN01		
					SIN1_1		
					FRCK0_2		
					TIOB8_1		
					INT02_1		
					WKUP1		
					MAD09_0		
64	54	J8	44	J8	P12	F	L
					AN02		
					SOT1_1 (SDA1_1)		
					IC00_2		
					TIOB9_1		
					MAD10_0		
-	-	K10	-	K10	VSS	-	
-	-	J9	-	J9	VSS	-	

Pin No					Pin Name	I/O Circuit Type	Pin State Type
LQFP-120	LQFP-100	BGA-112	LQFP-80	BGA-96			
65	55	H10	45	H10	P13	F	L
					AN03		
					SCK1_1 (SCL1_1)		
					IC01_2		
					TIOB10_1		
					RTCCO_1		
					SUBOUT_1		
					MAD11_0		
66	56	H9	46	H9	P14	F	M
					AN04		
					SIN0_1		
					IC02_2		
					TIOB11_1		
					INT03_1		
					MAD12_0		
67	57	H7	47	G10	P15	F	M
					AN05		
					SOT0_1 (SDA0_1)		
					IC03_2		
					TIOB12_1		
					INT14_0		
					MAD13_0		

Pin No					Pin Name	I/O Circuit Type	Pin State Type
LQFP-120	LQFP-100	BGA-112	LQFP-80	BGA-96			
68	58	G10	48	G9	P16 AN06 SCK0_1 (SCL0_1) TIOB13_1 INT15_0 MAD14_0	F	M
69	59	G9	49	F10	P17 AN07 SIN2_2 INT04_1 MAD15_0	F	M
70	60	H11	50	H11	AVCC	-	
71	61	F11	51	F11	AVRH	-	
72	62	G11	52	G11	AVSS	-	
73	63	G8	53	F9	P18 AN08 SOT2_2 (SDA2_2) TIOA8_1 MAD16_0	F	L
74	64	F10	54	E11	P19 AN09 SCK2_2 (SCL2_2) TIOA9_1 MAD17_0	F	L
-	-	H8	-	-	VSS	-	
75	65	F9	55	E10	P1A AN10 SIN4_1 IC00_1 TIOA10_1 INT05_1 MAD18_0	F	M

Pin No					Pin Name	I/O Circuit Type	Pin State Type
LQFP-120	LQFP-100	BGA-112	LQFP-80	BGA-96			
76	66	E11	56	E9	P1B AN11 SOT4_1 (SDA4_1) IC01_1 TIOA11_1 INT20_2 MAD19_0	F	M
77	67	E10	-	-	P1C AN12 SCK4_1 (SCL4_1) IC02_1 TIOA12_1 INT21_2 MAD20_0	F	M
78	68	F8	-	-	P1D AN13 CTS4_1 IC03_1 TIOA13_1 INT22_2 MAD21_0	F	M
79	69	E9	-	-	P1E AN14 RTS4_1 DTTI0X_1 TIOA9_2 INT23_2 MAD22_0	F	M
80	70	D11	-	-	P1F AN15 ADTG_5 FRCK0_1 TIOB9_2 MAD23_0	F	L
	-	-	-	-	SCK15_0 (SCL15_0)		
-	-	B10	-	B10	VSS	-	

Pin No					Pin Name	I/O Circuit Type	Pin State Type
LQFP-120	LQFP-100	BGA-112	LQFP-80	BGA-96			
-	-	C9	-	C9	VSS	-	
-	-	-	-	D11	VSS	-	
81	-	-	-	-	P28 ADTG_4 SOT15_0 (SDA15_0) RTO05_1 TIOB6_2	E	J
82	-	-	-	-	P27 SIN15_0 RTO04_1 TIOA6_2 INT02_2	E	K
83	-	-	-	-	P26 SCK2_1 (SCL2_1) RTO03_1 TIOA11_2	E	J
84	-	-	-	-	P25 SOT2_1 (SDA2_1) RTO02_1 TIOA14_1 TIOB11_2	E	J
85	-	-	-	-	P24 SIN2_1 RTO01_1 TIOB14_1 INT01_2	E	K
86	71	D10	57	D10	P23 AN16 SCK0_0 (SCL0_0) TIOA7_1	F	L
	-	-	-	-	RTO00_1		

Pin No					Pin Name	I/O Circuit Type	Pin State Type
LQFP-120	LQFP-100	BGA-112	LQFP-80	BGA-96			
87	72	E8	58	D9	P22	F	L
					AN17		
					SOT0_0 (SDA0_0)		
					ZIN1_1		
					TIOB7_1		
88	73	C11	59	C11	P21	F	P
					AN18		
					SIN0_0		
					BIN1_1		
					TIOB10_2		
					INT06_1		
					WKUP2		
89	74	C10	60	C10	P20	F	M
					AN19		
					CROUT_0		
					AIN1_1		
					TIOA10_2		
					INT05_0		
					MAD24_0		
90	75	A11	-	A11	VSS	-	
91	76	A10	-	-	VCC	-	
92	77	A9	61	A10	P00	E	I
					TRSTX		
					TIOA14_2		
					MCSX7_0		
			-	-	SCK8_0 (SCL8_0)		
93	78	B9	62	B9	P01	E	I
					TCK		
					SWCLK		
94	79	B11	63	B11	P02	E	I
					TDI		
					TIOB14_2		
					MCSX6_0		
			-	-	SOT8_0		

Pin No					Pin Name	I/O Circuit Type	Pin State Type
LQFP-120	LQFP-100	BGA-112	LQFP-80	BGA-96			
95	80	A8	64	A9	P03 TMS SWDIO	E	I
96	81	B8	65	B8	P04 TDO SWO	E	I
97	82	C8	-	-	P05 AN20 TRACED0 SIN8_0 SIN4_2 TIOA5_2 INT00_1 MCSX5_0	F	O
-	-	D8	-	-	VSS	-	
98	83	D9	-	-	P06 AN21 TRACED1 SOT4_2 (SDA4_2) TIOB5_2 INT01_1 MCSX4_0	F	O
99	84	A7	66	A8	P07 AN22 ADTG_0 MCLKOUT_0 INT23_1	F	O
			-	-	TRACED2 SCK4_2 (SCL4_2)		
-	-	-	-	A7	VSS	-	

Pin No					Pin Name	I/O Circuit Type	Pin State Type
LQFP-120	LQFP-100	BGA-112	LQFP-80	BGA-96			
100	85	B7	-	-	P08 AN23 TRACED3 CTS4_2 TIOA0_2 INT16_0 MCSX3_0	F	O
101	86	C7	-	-	P09 TRACECLK RTS4_2 TIOB0_2 INT17_0 MCSX2_0	E	N
102	87	D7	67	C8	P0A SIN4_0 INT00_2 WKUP5 MCSX1_0	H[1]	S
103	88	A6	68	C7	P0B SOT4_0 (SDA4_0) TIOB6_1 INT18_0 CEC0_1 MCSX0_0	H[1]	R
104	89	B6	69	B7	P0C SCK4_0 (SCL4_0) TIOA6_1 INT19_0 MALE_0	H[1]	K
-	-	D4	-	-	VSS	-	

Pin No					Pin Name	I/O Circuit Type	Pin State Type
LQFP-120	LQFP-100	BGA-112	LQFP-80	BGA-96			
-	-	C3	-	C3	VSS	-	
105	90	C6	70	B6	P0D RTS4_0 TIOA3_2 INT20_0 MDQM0_0	E	K
106	91	A5	71	C6	P0E CTS4_0 TIOB3_2 INT21_0 MDQM1_0	E	K
-	-	-	-	A5	VSS	-	
107	92	B5	72	A6	P0F NMIX CROUT_1 RTCCO_0 SUBOUT_0 WKUP0	E	H
108	-	-	-	-	P68 SCK3_0 (SCL3_0) TIOB7_2 INT12_2	E	K
109	-	-	-	-	P67 SOT3_0 (SDA3_0) TIOA7_2 INT22_0	E	K
110	-	-	-	-	P66 SIN3_0 TIOA12_2 INT11_2	E	K

Pin No					Pin Name	I/O Circuit Type	Pin State Type
LQFP-120	LQFP-100	BGA-112	LQFP-80	BGA-96			
111	-	-	-	-	P65	E	K
					SCK5_1 (SCL5_1)		
					TIOB7_0		
					TIOB12_2		
					INT23_0		
112	-	-	-	-	P64	E	K
					SOT5_1 (SDA5_1)		
					TIOA7_0		
					INT10_2		
113	93	D6	73	B5	P63	E	K
					TIOB15_1		
					INT03_0		
					MWEX_0		
	-	-	-	-	SIN5_1		
114	94	C5	74	C5	P62	E	K
					ADTG_3		
					SCK5_0 (SCL5_0)		
					TIOA15_1		
					INT07_1		
					MOEX_0		
115	95	B4	75	B4	P61	E	J
					SOT5_0 (SDA5_0)		
					TIOB2_2		
116	96	C4	76	C4	P60	H[1]	Q
					SIN5_0		
					IGTRG_1		
					TIOA2_2		
					INT15_1		
					WKUP3		
					CEC1_0		
					MRDY_0		

Pin No					Pin Name	I/O Circuit Type	Pin State Type
LQFP-120	LQFP-100	BGA-112	LQFP-80	BGA-96			
117	97	A4	77	A4	VCC	-	
118	98	A3	78	A3	P80	E	K
					TIOB15_0		
					INT16_1		
119	99	A2	79	A2	P81	E	K
					TIOA15_0		
					INT17_1		
120	100	A1	80	A1	VSS	-	

[1]. 5V tolerant I/O

4.2 List of Pin Functions

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

Pin Function	Pin Name	Function Description	Pin No				
			LQFP-120	LQFP-100	BGA-112	LQFP-80	BGA-96
ADC	ADTG_0	A/D converter external trigger input pin	99	84	A7	66	A8
	ADTG_1		7	7	D3	7	D3
	ADTG_2		23	18	F4	13	G3
	ADTG_3		114	94	C5	74	C5
	ADTG_4		81	-	-	-	-
	ADTG_5		80	70	D11	-	-
	ADTG_6		17	12	E4	12	G2
	ADTG_7		35	30	J5	-	-
	ADTG_8		-	-	-	-	-
	AN00	A/D converter analog input pin. ANxx describes ADC ch.xx.	62	52	J11	42	J11
	AN01		63	53	J10	43	J10
	AN02		64	54	J8	44	J8
	AN03		65	55	H10	45	H10
	AN04		66	56	H9	46	H9
	AN05		67	57	H7	47	G10
	AN06		68	58	G10	48	G9
	AN07		69	59	G9	49	F10
	AN08		73	63	G8	53	F9
	AN09		74	64	F10	54	E11
	AN10		75	65	F9	55	E10
	AN11		76	66	E11	56	E9
	AN12		77	67	E10	-	-
	AN13		78	68	F8	-	-
	AN14		79	69	E9	-	-
	AN15		80	70	D11	-	-
	AN16		86	71	D10	57	D10
	AN17		87	72	E8	58	D9
	AN18		88	73	C11	59	C11
	AN19		89	74	C10	60	C10
	AN20		97	82	C8	-	-
	AN21		98	83	D9	-	-
	AN22		99	84	A7	66	A8
	AN23		100	85	B7	-	-

Pin Function	Pin Name	Function Description	Pin No				
			LQFP-120	LQFP-100	BGA-112	LQFP-80	BGA-96
Base Timer 0	TIOA0_0	Base timer ch.0 TIOA pin	32	27	J4	-	-
	TIOA0_1		24	19	G3	14	H1
	TIOA0_2		100	85	B7	-	-
	TIOB0_0	Base timer ch.0 TIOB pin	45	40	J6	30	K6
	TIOB0_1		14	9	E1	9	E2
	TIOB0_2		101	86	C7	-	-
Base Timer 1	TIOA1_0	Base timer ch.1 TIOA pin	33	28	L5	-	-
	TIOA1_1		25	20	H1	15	H2
	TIOA1_2		5	5	D1	5	D1
	TIOB1_0	Base timer ch.1 TIOB pin	46	41	L7	31	J6
	TIOB1_1		15	10	E2	10	E3
	TIOB1_2		6	6	D2	6	D2
Base Timer 2	TIOA2_0	Base timer ch.2 TIOA pin	34	29	K5	-	-
	TIOA2_1		26	21	H2	16	H3
	TIOA2_2		116	96	C4	76	C4
	TIOB2_0	Base timer ch.2 TIOB pin	47	42	K7	32	L7
	TIOB2_1		16	11	E3	11	G1
	TIOB2_2		115	95	B4	75	B4
Base Timer 3	TIOA3_0	Base timer ch.3 TIOA pin	35	30	J5	-	-
	TIOA3_1		27	22	G4	17	J1
	TIOA3_2		105	90	C6	70	B6
	TIOB3_0	Base timer ch.3 TIOB pin	48	43	H6	33	K7
	TIOB3_1		17	12	E4	12	G2
	TIOB3_2		106	91	A5	71	C6
Base Timer 4	TIOA4_0	Base timer ch.4 TIOA pin	36	31	H5	21	L5
	TIOA4_1		28	23	H3	18	J2
	TIOA4_2		51	-	-	-	-
	TIOB4_0	Base timer ch.4 TIOB pin	49	44	J7	34	J7
	TIOB4_1		18	13	F1	-	-
	TIOB4_2		52	-	-	-	-
Base Timer 5	TIOA5_0	Base timer ch.5 TIOA pin	37	32	L6	22	K5
	TIOA5_1		29	24	J2	19	J4
	TIOA5_2		97	82	C8	-	-
	TIOB5_0	Base timer ch.5 TIOB pin	50	45	K8	35	K8
	TIOB5_1		19	14	F2	-	-
	TIOB5_2		98	83	D9	-	-

Pin Function	Pin Name	Function Description	Pin No				
			LQFP-120	LQFP-100	BGA-112	LQFP-80	BGA-96
Base Timer 6	TIOA6_0	Base timer ch.6 TIOA pin	53	-	-	-	-
	TIOA6_1		104	89	B6	69	B7
	TIOA6_2		82	-	-	-	-
	TIOB6_0	Base timer ch.6 TIOB pin	54	-	-	-	-
	TIOB6_1		103	88	A6	68	C7
	TIOB6_2		81	-	-	-	-
Base Timer 7	TIOA7_0	Base timer ch.7 TIOA pin	112	-	-	-	-
	TIOA7_1		86	71	D10	57	D10
	TIOA7_2		109	-	-	-	-
	TIOB7_0	Base timer ch.7 TIOB pin	111	-	-	-	-
	TIOB7_1		87	72	E8	58	D9
	TIOB7_2		108	-	-	-	-
Base Timer 8	TIOA8_0	Base timer ch.8 TIOA pin	8	8	D5	8	E1
	TIOA8_1		73	63	G8	53	F9
	TIOA8_2		22	17	G2	-	-
	TIOB8_0	Base timer ch.8 TIOB pin	2	2	C1	2	C1
	TIOB8_1		63	53	J10	43	J10
	TIOB8_2		23	18	F4	-	-
Base Timer 9	TIOA9_0	Base timer ch.9 TIOA pin	9	-	-	-	-
	TIOA9_1		74	64	F10	54	E11
	TIOA9_2		79	69	E9	-	-
	TIOB9_0	Base timer ch.9 TIOB pin	3	3	C2	3	C2
	TIOB9_1		64	54	J8	44	J8
	TIOB9_2		80	70	D11	-	-
Base Timer 10	TIOA10_0	Base timer ch.10 TIOA pin	10	-	-	-	-
	TIOA10_1		75	65	F9	55	E10
	TIOA10_2		89	74	C10	60	C10
	TIOB10_0	Base timer ch.10 TIOB pin	4	4	B3	4	B3
	TIOB10_1		65	55	H10	45	H10
	TIOB10_2		88	73	C11	59	C11
Base Timer 11	TIOA11_0	Base timer ch.11 TIOA pin	11	-	-	-	-
	TIOA11_1		76	66	E11	56	E9
	TIOA11_2		83	-	-	-	-
	TIOB11_0	Base timer ch.11 TIOB pin	5	5	D1	5	D1
	TIOB11_1		66	56	H9	46	H9
	TIOB11_2		84	-	-	-	-

Pin Function	Pin Name	Function Description	Pin No				
			LQFP-120	LQFP-100	BGA-112	LQFP-80	BGA-96
Base Timer 12	TIOA12_0	Base timer ch.12 TIOA pin	12	-	-	-	-
	TIOA12_1		77	67	E10	-	-
	TIOA12_2		110	-	-	-	-
	TIOB12_0	Base timer ch.12 TIOB pin	6	6	D2	6	D2
	TIOB12_1		67	57	H7	47	G10
	TIOB12_2		111	-	-	-	-
Base Timer 13	TIOA13_0	Base timer ch.13 TIOA pin	13	-	-	-	-
	TIOA13_1		78	68	F8	-	-
	TIOA13_2		14	9	E1	9	E2
	TIOB13_0	Base timer ch.13 TIOB pin	7	7	D3	7	D3
	TIOB13_1		68	58	G10	48	G9
	TIOB13_2		15	10	E2	10	E3
Base Timer 14	TIOA14_0	Base timer ch.14 TIOA pin	21	16	G1	-	-
	TIOA14_1		84	-	-	-	-
	TIOA14_2		92	77	A9	61	A10
	TIOB14_0	Base timer ch.14 TIOB pin	20	15	F3	-	-
	TIOB14_1		85	-	-	-	-
	TIOB14_2		94	79	B11	63	B11
Base Timer 15	TIOA15_0	Base timer ch.15 TIOA pin	119	99	A2	79	A2
	TIOA15_1		114	94	C5	74	C5
	TIOA15_2		18	13	F1	-	-
	TIOB15_0	Base timer ch.15 TIOB pin	118	98	A3	78	A3
	TIOB15_1		113	93	D6	73	B5
	TIOB15_2		19	14	F2	-	-

Pin Function	Pin Name	Function Description	Pin No				
			LQFP-120	LQFP-100	BGA-112	LQFP-80	BGA-96
Debugger	SWCLK	Serial wire debug interface clock input pin	93	78	B9	62	B9
	SWDIO	Serial wire debug interface data input / output pin	95	80	A8	64	A9
	SWO	Serial wire viewer output pin	96	81	B8	65	B8
	TCK	JTAG test clock input pin	93	78	B9	62	B9
	TDI	JTAG test data input pin	94	79	B11	63	B11
	TDO	JTAG debug data output pin	96	81	B8	65	B8
	TMS	JTAG test mode state input/output pin	95	80	A8	64	A9
	TRACECLK	Trace CLK output pin of ETM	101	86	C7	-	-
	TRACED0	Trace data output pin of ETM	97	82	C8	-	-
	TRACED1		98	83	D9	-	-
	TRACED2		99	84	A7	-	-
	TRACED3		100	85	B7	-	-
	TRSTX	JTAG test reset input pin	92	77	A9	61	A10
External Bus	MAD00_0	External bus interface address bus	36	31	H5	21	L5
	MAD01_0		37	32	L6	22	K5
	MAD02_0		44	39	K6	29	J5
	MAD03_0		45	40	J6	30	K6
	MAD04_0		46	41	L7	31	J6
	MAD05_0		47	42	K7	32	L7
	MAD06_0		48	43	H6	33	K7
	MAD07_0		49	44	J7	34	J7
	MAD08_0		50	45	K8	35	K8
	MAD09_0		63	53	J10	43	J10
	MAD10_0		64	54	J8	44	J8
	MAD11_0		65	55	H10	45	H10
	MAD12_0		66	56	H9	46	H9
	MAD13_0		67	57	H7	47	G10
	MAD14_0		68	58	G10	48	G9
	MAD15_0		69	59	G9	49	F10
	MAD16_0		73	63	G8	53	F9
	MAD17_0		74	64	F10	54	E11
	MAD18_0		75	65	F9	55	E10
	MAD19_0		76	66	E11	56	E9
	MAD20_0		77	67	E10	-	-
	MAD21_0		78	68	F8	-	-
	MAD22_0		79	69	E9	-	-
	MAD23_0		80	70	D11	-	-
	MAD24_0		89	74	C10	60	C10

Pin Function	Pin Name	Function Description	Pin No				
			LQFP-120	LQFP-100	BGA-112	LQFP-80	BGA-96
External Bus	MCSX0_0	External bus interface chip select output pin	103	88	A6	68	C7
	MCSX1_0		102	87	D7	67	C8
	MCSX2_0		101	86	C7	-	-
	MCSX3_0		100	85	B7	-	-
	MCSX4_0		98	83	D9	-	-
	MCSX5_0		97	82	C8	-	-
	MCSX6_0		94	79	B11	63	B11
	MCSX7_0		92	77	A9	61	A10
	MDQM0_0	External bus interface byte mask signal output pin	105	90	C6	70	B6
	MDQM1_0		106	91	A5	71	C6
	MOEX_0	External bus interface read enable signal for SRAM	114	94	C5	74	C5
	MWEX_0	External bus interface write enable signal for SRAM	113	93	D6	73	B5
	MNALE_0	External bus interface ALE signal to control NAND Flash memory output pin	18	-	-	-	-
	MNCLE_0	External bus interface CLE signal to control NAND Flash memory output pin	19	-	-	-	-
	MNREX_0	External bus interface read enable signal to control NAND Flash memory	21	-	-	-	-
	MNWEX_0	External bus interface write enable signal to control NAND Flash memory	20	-	-	-	-
	MADATA00_0	External bus interface data bus	2	2	C1	2	C1
	MADATA01_0		3	3	C2	3	C2
	MADATA02_0		4	4	B3	4	B3
	MADATA03_0		5	5	D1	5	D1
	MADATA04_0		6	6	D2	6	D2
	MADATA05_0		7	7	D3	7	D3
	MADATA06_0		8	8	D5	8	E1
	MADATA07_0		9	9	E1	9	E2
	MADATA08_0		10	10	E2	10	E3
	MADATA09_0		11	11	E3	11	G1
	MADATA10_0		12	12	E4	12	G2
	MADATA11_0		13	13	F1	-	-
	MADATA12_0		14	14	F2	-	-

Pin Function	Pin Name	Function Description	Pin No				
			LQFP-120	LQFP-100	BGA-112	LQFP-80	BGA-96
External Bus	MADATA13_0		15	15	F3	-	-
	MADATA14_0		16	16	G1	-	-
	MADATA15_0		17	17	G2	-	-
	MALE_0	Latch enable signal for multiplex	104	89	B6	69	B7
	MRDY_0	External RDY input signal	116	96	C4	76	C4
	MCLKOUT_0	External bus clock output pin	99	84	A7	66	A8
External Interrupt	INT00_0	External interrupt request 00 input pin	2	2	C1	2	C1
	INT00_1		97	82	C8	-	-
	INT00_2		102	87	D7	67	C8
	INT01_0	External interrupt request 01 input pin	3	3	C2	3	C2
	INT01_1		98	83	D9	-	-
	INT01_2		85	-	-	-	-
	INT02_0	External interrupt request 02 input pin	4	4	B3	4	B3
	INT02_1		63	53	J10	43	J10
	INT02_2		82	-	-	-	-
	INT03_0	External interrupt request 03 input pin	113	93	D6	73	B5
	INT03_1		66	56	H9	46	H9
	INT03_2		14	9	E1	9	E2
	INT04_0	External interrupt request 04 input pin	17	12	E4	12	G2
	INT04_1		69	59	G9	49	F10
	INT04_2		15	10	E2	10	E3
	INT05_0	External interrupt request 05 input pin	89	74	C10	60	C10
	INT05_1		75	65	F9	55	E10
	INT05_2		16	11	E3	11	G1
	INT06_0	External interrupt request 06 input pin	23	18	F4	13	G3
	INT06_1		88	73	C11	59	C11
	INT06_2		50	45	K8	35	K8
	INT07_0	External interrupt request 07 input pin	24	19	G3	14	H1
	INT07_1		114	94	C5	74	C5
	INT07_2		5	5	D1	5	D1
	INT08_0	External interrupt request 08 input pin	34	29	K5	-	-
	INT08_1		19	14	F2	-	-
	INT08_2		8	8	D5	8	E1
	INT09_0	External interrupt request 09 input pin	35	30	J5	-	-
	INT09_1		20	15	F3	-	-
	INT09_2		11	-	-	-	-
	INT10_0	External interrupt request 10 input pin	36	31	H5	21	L5
	INT10_1		21	16	G1	-	-
	INT10_2		112	-	-	-	-
	INT11_0	External interrupt request 11 input pin	37	32	L6	22	K5
	INT11_1		22	17	G2	-	-
	INT11_2		110	-	-	-	-

Pin Function	Pin Name	Function Description	Pin No				
			LQFP-120	LQFP-100	BGA-112	LQFP-80	BGA-96
External Interrupt	INT12_0	External interrupt request 12 input pin	48	43	H6	33	K7
	INT12_1		32	27	J4	-	-
	INT12_2		108	-	-	-	-
	INT13_0	External interrupt request 13 input pin	49	44	J7	34	J7
	INT13_1		33	28	L5	-	-
	INT13_2		52	-	-	-	-
	INT14_0	External interrupt request 14 input pin	67	57	H7	47	G10
	INT14_1		44	39	K6	29	J5
	INT14_2		53	-	-	-	-
	INT15_0	External interrupt request 15 input pin	68	58	G10	48	G9
	INT15_1		116	96	C4	76	C4
	INT15_2		54	-	-	-	-
	INT16_0	External interrupt request 16 input pin	100	85	B7	-	-
	INT16_1		118	98	A3	78	A3
	INT16_2		12	-	-	-	-
	INT17_0	External interrupt request 17 input pin	101	86	C7	-	-
	INT17_1		119	99	A2	79	A2
	INT17_2		13	-	-	-	-
	INT18_0	External interrupt request 18 input pin	103	88	A6	68	C7
	INT18_1		6	6	D2	6	D2
	INT18_2		26	21	H2	16	H3
	INT19_0	External interrupt request 19 input pin	104	89	B6	69	B7
	INT19_1		7	7	D3	7	D3
	INT19_2		28	23	H3	18	J2
	INT20_0	External interrupt request 20 input pin	105	90	C6	70	B6
	INT20_1		45	40	J6	30	K6
	INT20_2		76	66	E11	56	E9
	INT21_0	External interrupt request 21 input pin	106	91	A5	71	C6
	INT21_1		46	41	L7	31	J6
	INT21_2		77	67	E10	-	-
	INT22_0	External interrupt request 22 input pin	109	-	-	-	-
	INT22_1		47	42	K7	32	L7
	INT22_2		78	68	F8	-	-
	INT23_0	External interrupt request 23 input pin	111	-	-	-	-
	INT23_1		99	84	A7	66	A8
	INT23_2		79	69	E9	-	-
	NMIX	Non-Maskable Interrupt input pin	107	92	B5	72	A6

Pin Function	Pin Name	Function Description	Pin No				
			LQFP-120	LQFP-100	BGA-112	LQFP-80	BGA-96
GPIO	P00	General-purpose I/O port 0	92	77	A9	61	A10
	P01		93	78	B9	62	B9
	P02		94	79	B11	63	B11
	P03		95	80	A8	64	A9
	P04		96	81	B8	65	B8
	P05		97	82	C8	-	-
	P06		98	83	D9	-	-
	P07		99	84	A7	66	A8
	P08		100	85	B7	-	-
	P09		101	86	C7	-	-
	P0A		102	87	D7	67	C8
	P0B		103	88	A6	68	C7
	P0C		104	89	B6	69	B7
	P0D		105	90	C6	70	B6
	P0E		106	91	A5	71	C6
	P0F		107	92	B5	72	A6
	P10	General-purpose I/O port 1	62	52	J11	42	J11
	P11		63	53	J10	43	J10
	P12		64	54	J8	44	J8
	P13		65	55	H10	45	H10
	P14		66	56	H9	46	H9
	P15		67	57	H7	47	G10
	P16		68	58	G10	48	G9
	P17		69	59	G9	49	F10
	P18		73	63	G8	53	F9
	P19		74	64	F10	54	E11
	P1A		75	65	F9	55	E10
	P1B		76	66	E11	56	E9
	P1C		77	67	E10	-	-
	P1D		78	68	F8	-	-
	P1E		79	69	E9	-	-
	P1F		80	70	D11	-	-
	P20	General-purpose I/O port 2	89	74	C10	60	C10
	P21		88	73	C11	59	C11
	P22		87	72	E8	58	D9
	P23		86	71	D10	57	D10
	P24		85	-	-	-	-
	P25		84	-	-	-	-
	P26		83	-	-	-	-
	P27		82	-	-	-	-
	P28		81	-	-	-	-

Pin Function	Pin Name	Function Description	Pin No				
			LQFP-120	LQFP-100	BGA-112	LQFP-80	BGA-96
GPIO	P30	General-purpose I/O port 3	14	9	E1	9	E2
	P31		15	10	E2	10	E3
	P32		16	11	E3	11	G1
	P33		17	12	E4	12	G2
	P34		18	13	F1	-	-
	P35		19	14	F2	-	-
	P36		20	15	F3	-	-
	P37		21	16	G1	-	-
	P38		22	17	G2	-	-
	P39		23	18	F4	13	G3
	P3A		24	19	G3	14	H1
	P3B		25	20	H1	15	H2
	P3C		26	21	H2	16	H3
	P3D		27	22	G4	17	J1
	P3E		28	23	H3	18	J2
	P3F		29	24	J2	19	J4
	P40	General-purpose I/O port 4	32	27	J4	-	-
	P41		33	28	L5	-	-
	P42		34	29	K5	-	-
	P43		35	30	J5	-	-
	P44		36	31	H5	21	L5
	P45		37	32	L6	22	K5
	P46		41	36	L3	26	L3
	P47		42	37	K3	27	K3
	P48		44	39	K6	29	J5
	P49		45	40	J6	30	K6
	P4A		46	41	L7	31	J6
	P4B		47	42	K7	32	L7
	P4C		48	43	H6	33	K7
	P4D		49	44	J7	34	J7
	P4E		50	45	K8	35	K8
	P50	General-purpose I/O port 5	2	2	C1	2	C1
	P51		3	3	C2	3	C2
	P52		4	4	B3	4	B3
	P53		5	5	D1	5	D1
	P54		6	6	D2	6	D2
	P55		7	7	D3	7	D3
	P56		8	8	D5	8	E1
	P57		9	-	-	-	-
	P58		10	-	-	-	-
	P59		11	-	-	-	-
	P5A		12	-	-	-	-
	P5B		13	-	-	-	-

Pin Function	Pin Name	Function Description	Pin No				
			LQFP-120	LQFP-100	BGA-112	LQFP-80	BGA-96
GPIO	P60	General-purpose I/O port 6	116	96	C4	76	C4
	P61		115	95	B4	75	B4
	P62		114	94	C5	74	C5
	P63		113	93	D6	73	B5
	P64		112	-	-	-	-
	P65		111	-	-	-	-
	P66		110	-	-	-	-
	P67		109	-	-	-	-
	P68		108	-	-	-	-
	P70	General-purpose I/O port 7	51	-	-	-	-
	P71		52	-	-	-	-
	P72		53	-	-	-	-
	P73		54	-	-	-	-
	P74		55	-	-	-	-
	P80	General-purpose I/O port 8	118	98	A3	78	A3
	P81		119	99	A2	79	A2
	PE0	General-purpose I/O port E	56	46	K9	36	K9
	PE2		58	48	L9	38	L9
	PE3		59	49	L10	39	L10

Pin Function	Pin Name	Function Description	Pin No				
			LQFP-120	LQFP-100	BGA-112	LQFP-80	BGA-96
Multi- function Serial 0	SIN0_0	Multi-function serial interface ch.0 input pin	88	73	C11	59	C11
	SIN0_1		66	56	H9	46	H9
	SOT0_0 (SDA0_0)	Multi-function serial interface ch.0 output pin. This pin operates as SOT0 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA0 when it is used in an I^2C (operation mode 4).	87	72	E8	58	D9
	SOT0_1 (SDA0_1)		67	57	H7	47	G10
	SCK0_0 (SCL0_0)	Multi-function serial interface ch.0 clock I/O pin. This pin operates as SCK0 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL0 when it is used in an I^2C (operation mode 4).	86	71	D10	57	D10
	SCK0_1 (SCL0_1)		68	58	G10	48	G9
Multi- function Serial 1	SIN1_0	Multi-function serial interface ch.1 input pin	8	-	-	-	-
	SIN1_1		63	53	J10	43	J10
	SOT1_0 (SDA1_0)	Multi-function serial interface ch.1 output pin. This pin operates as SOT1 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA1 when it is used in an I^2C (operation mode 4).	9	-	-	-	-
	SOT1_1 (SDA1_1)		64	54	J8	44	J8
	SCK1_0 (SCL1_0)	Multi-function serial interface ch.1 clock I/O pin. This pin operates as SCK1 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL1 when it is used in an I^2C (operation mode 4).	10	-	-	-	-
	SCK1_1 (SCL1_1)		65	55	H10	45	H10

Pin Function	Pin Name	Function Description	Pin No				
			LQFP-120	LQFP-100	BGA-112	LQFP-80	BGA-96
Multi- function Serial 2	SIN2_0	Multi-function serial interface ch.2 input pin	53	-	-	-	-
	SIN2_1		85	-	-	-	-
	SIN2_2		69	59	G9	49	F10
	SOT2_0 (SDA2_0)	Multi-function serial interface ch.2 output pin. This pin operates as SOT2 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA2 when it is used in an I^2C (operation mode 4).	54	-	-	-	-
	SOT2_1 (SDA2_1)		84	-	-	-	-
	SOT2_2 (SDA2_2)		73	63	G8	53	F9
	SCK2_0 (SCL2_0)	Multi-function serial interface ch.2 clock I/O pin. This pin operates as SCK2 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL2 when it is used in an I^2C (operation mode 4).	55	-	-	-	-
	SCK2_1 (SCL2_1)		83	-	-	-	-
	SCK2_2 (SCL2_2)		74	64	F10	54	E11
Multi- function Serial 3	SIN3_0	Multi-function serial interface ch.3 input pin	110	-	-	-	-
	SIN3_1		2	2	C1	2	C1
	SIN3_2		44	39	K6	29	J5
	SOT3_0 (SDA3_0)	Multi-function serial interface ch.3 output pin. This pin operates as SOT3 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA3 when it is used in an I^2C (operation mode 4).	109	-	-	-	-
	SOT3_1 (SDA3_1)		3	3	C2	3	C2
	SOT3_2 (SDA3_2)		45	40	J6	30	K6
	SCK3_0 (SCL3_0)	Multi-function serial interface ch.3 clock I/O pin. This pin operates as SCK3 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL3 when it is used in an I^2C (operation mode 4).	108	-	-	-	-
	SCK3_1 (SCL3_1)		4	4	B3	4	B3
	SCK3_2 (SCL3_2)		46	41	L7	31	J6

Pin Function	Pin Name	Function Description	Pin No				
			LQFP-120	LQFP-100	BGA-112	LQFP-80	BGA-96
Multi- function Serial 4	SIN4_0	Multi-function serial interface ch.4 input pin	102	87	D7	67	C8
	SIN4_1		75	65	F9	55	E10
	SIN4_2		97	82	C8	-	-
	SOT4_0 (SDA4_0)	Multi-function serial interface ch.4 output pin. This pin operates as SOT4 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA4 when it is used in an I^2C (operation mode 4).	103	88	A6	68	C7
	SOT4_1 (SDA4_1)		76	66	E11	56	E9
	SOT4_2 (SDA4_2)		98	83	D9	-	-
	SCK4_0 (SCL4_0)	Multi-function serial interface ch.4 clock I/O pin. This pin operates as SCK4 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL4 when it is used in an I^2C (operation mode 4).	104	89	B6	69	B7
	SCK4_1 (SCL4_1)		77	67	E10	-	-
	SCK4_2 (SCL4_2)		99	84	A7	-	-
	RTS4_0	Multi-function serial interface ch.4 RTS output pin	105	90	C6	70	B6
	RTS4_1		79	69	E9	-	-
	RTS4_2		101	86	C7	-	-
	CTS4_0	Multi-function serial interface ch.4 CTS input pin	106	91	A5	71	C6
	CTS4_1		78	68	F8	-	-
	CTS4_2		100	85	B7	-	-
Multi- function Serial 5	SIN5_0	Multi-function serial interface ch.5 input pin	116	96	C4	76	C4
	SIN5_1		113	-	-	-	-
	SIN5_2		20	15	F3	-	-
	SOT5_0 (SDA5_0)	Multi-function serial interface ch.5 output pin. This pin operates as SOT5 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA5 when it is used in an I^2C (operation mode 4).	115	95	B4	75	B4
	SOT5_1 (SDA5_1)		112	-	-	-	-
	SOT5_2 (SDA5_2)		21	16	G1	-	-
	SCK5_0 (SCL5_0)	Multi-function serial interface ch.5 clock I/O pin. This pin operates as SCK5 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL5 when it is used in an I^2C (operation mode 4).	114	94	C5	74	C5
	SCK5_1 (SCL5_1)		111	-	-	-	-
	SCK5_2 (SCL5_2)		22	17	G2	-	-

Pin Function	Pin Name	Function Description	Pin No				
			LQFP-120	LQFP-100	BGA-112	LQFP-80	BGA-96
Multi- function Serial 6	SIN6_0	Multi-function serial interface ch.6 input pin	5	5	D1	5	D1
	SIN6_1		17	12	E4	12	G2
	SOT6_0 (SDA6_0)	Multi-function serial interface ch.6 output pin. This pin operates as SOT6 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA6 when it is used in an I^2C (operation mode 4).	6	6	D2	6	D2
	SOT6_1 (SDA6_1)		16	11	E3	11	G1
	SCK6_0 (SCL6_0)	Multi-function serial interface ch.6 clock I/O pin. This pin operates as SCK6 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL6 when it is used in an I^2C (operation mode 4).	7	7	D3	7	D3
	SCK6_1 (SCL6_1)		15	10	E2	10	E3
Multi- function Serial 7	SIN7_0	Multi-function serial interface ch.7 input pin	11	-	-	-	-
	SIN7_1		50	45	K8	35	K8
	SOT7_0 (SDA7_0)	Multi-function serial interface ch.7 output pin. This pin operates as SOT7 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA7 when it is used in an I^2C (operation mode 4).	12	-	-	-	-
	SOT7_1 (SDA7_1)		49	44	J7	34	J7
	SCK7_0 (SCL7_0)	Multi-function serial interface ch.7 clock I/O pin. This pin operates as SCK7 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL7 when it is used in an I^2C (operation mode 4).	13	-	-	-	-
	SCK7_1 (SCL7_1)		48	43	H6	33	K7

Pin Function	Pin Name	Function Description	Pin No				
			LQFP-120	LQFP-100	BGA-112	LQFP-80	BGA-96
Multi- function Serial 8	SIN8_0	Multi-function serial interface ch.8 input pin	97	82	C8	-	-
	SOT8_0 (SDA8_0)	Multi-function serial interface ch.8 output pin. This pin operates as SOT8 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA8 when it is used in an I^2C (operation mode 4).	94	79	B11	-	-
	SCK8_0 (SCL8_0)	Multi-function serial interface ch.8 clock I/O pin. This pin operates as SCK8 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL8 when it is used in an I^2C (operation mode 4).	92	77	A9	-	-
Multi- function Serial 9	SIN9_0	Multi-function serial interface ch.9 input pin	17	12	E4	-	-
	SOT9_0 (SDA9_0)	Multi-function serial interface ch.9 output pin. This pin operates as SOT9 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA9 when it is used in an I^2C (operation mode 4).	18	13	F1	-	-
	SCK9_0 (SCL9_0)	Multi-function serial interface ch.9 clock I/O pin. This pin operates as SCK9 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL9 when it is used in an I^2C (operation mode 4).	19	14	F2	-	-

Pin Function	Pin Name	Function Description	Pin No				
			LQFP-120	LQFP-100	BGA-112	LQFP-80	BGA-96
Multi- function Serial 10	SIN10_0	Multi-function serial interface ch.10 input pin	23	18	F4	13	G3
	SOT10_0 (SDA10_0)	Multi-function serial interface ch.10 output pin. This pin operates as SOT10 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA10 when it is used in an I^2C (operation mode 4).	24	19	G3	14	H1
	SCK10_0 (SCL10_0)	Multi-function serial interface ch.10 clock I/O pin. This pin operates as SCK10 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL10 when it is used in an I^2C (operation mode 4).	25	20	H1	15	H2
Multi- function Serial 11	SIN11_0	Multi-function serial interface ch.11 input pin	26	21	H2	16	H3
	SOT11_0 (SDA11_0)	Multi-function serial interface ch.11 output pin. This pin operates as SOT11 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA11 when it is used in an I^2C (operation mode 4).	27	22	G4	17	J1
	SCK11_0 (SCL11_0)	Multi-function serial interface ch.11 clock I/O pin. This pin operates as SCK11 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL11 when it is used in an I^2C (operation mode 4).	28	23	H3	18	J2

Pin Function	Pin Name	Function Description	Pin No				
			LQFP-120	LQFP-100	BGA-112	LQFP-80	BGA-96
Multi- function Serial 12	SIN12_0	Multi-function serial interface ch.12 input pin	32	27	J4	-	-
	SOT12_0 (SDA12_0)	Multi-function serial interface ch.12 output pin. This pin operates as SOT12 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA12 when it is used in an I^2C (operation mode 4).	33	28	L5	-	-
	SCK12_0 (SCL12_0)	Multi-function serial interface ch.12 clock I/O pin. This pin operates as SCK12 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL12 when it is used in an I^2C (operation mode 4).	34	29	K5	-	-
Multi- function Serial 13	SIN13_0	Multi-function serial interface ch.13 input pin	35	30	J5	-	-
	SOT13_0 (SDA13_0)	Multi-function serial interface ch.13 output pin. This pin operates as SOT13 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA13 when it is used in an I^2C (operation mode 4).	36	31	H5	-	-
	SCK13_0 (SCL13_0)	Multi-function serial interface ch.13 clock I/O pin. This pin operates as SCK13 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL13 when it is used in an I^2C (operation mode 4).	37	32	L6	-	-

Pin Function	Pin Name	Function Description	Pin No				
			LQFP-120	LQFP-100	BGA-112	LQFP-80	BGA-96
Multi- function Serial 14	SIN14_0	Multi-function serial interface ch.14 input pin	50	-	-	-	-
	SOT14_0 (SDA14_0)	Multi-function serial interface ch.14 output pin. This pin operates as SOT14 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA14 when it is used in an I^2C (operation mode 4).	51	-	-	-	-
	SCK14_0 (SCL14_0)	Multi-function serial interface ch.14 clock I/O pin. This pin operates as SCK14 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL14 when it is used in an I^2C (operation mode 4).	52	-	-	-	-
Multi- function Serial 15	SIN15_0	Multi-function serial interface ch.15 input pin	82	-	-	-	
	SOT15_0 (SDA15_0)	Multi-function serial interface ch.15 output pin. This pin operates as SOT15 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA15 when it is used in an I^2C (operation mode 4).	81	-	-	-	
	SCK15_0 (SCL15_0)	Multi-function serial interface ch.15 clock I/O pin. This pin operates as SCK15 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL15 when it is used in an I^2C (operation mode 4).	80	-	-	-	

Pin Function	Pin Name	Function Description	Pin No				
			LQFP-120	LQFP-100	BGA-112	LQFP-80	BGA-96
Multi- function Timer 0	DTTI0X_0	Input signal of waveform generator to control outputs RTO00 to RTO05 of multi-function timer 0.	23	18	F4	13	G3
	DTTI0X_1		79	69	E9	-	-
	FRCK0_0	16-bit free-run timer ch.0 external clock input pin	18	13	F1	-	-
	FRCK0_1		80	70	D11	-	-
	FRCK0_2		63	53	J10	43	J10
	IC00_0	16-bit input capture input pin of multi-function timer 0. ICxx describes channel number.	22	17	G2	-	-
	IC00_1		75	65	F9	55	E10
	IC00_2		64	54	J8	44	J8
	IC01_0		21	16	G1	-	-
	IC01_1		76	66	E11	56	E9
	IC01_2		65	55	H10	45	H10
	IC02_0		20	15	F3	-	-
	IC02_1		77	67	E10	-	-
	IC02_2		66	56	H9	46	H9
	IC03_0		19	14	F2	-	-
	IC03_1		78	68	F8	-	-
	IC03_2		67	57	H7	47	G10

Pin Function	Pin Name	Function Description	Pin No				
			LQFP-120	LQFP-100	BGA-112	LQFP-80	BGA-96
Multi- function Timer 0	RTO00_0 (PPG00_0)	Waveform generator output pin of multi-function timer 0. This pin operates as PPG00 when it is used in PPG0 output mode.	24	19	G3	14	H1
	RTO00_1 (PPG00_1)		86	71	D10	57	D10
	RTO01_0 (PPG00_0)	Waveform generator output pin of multi-function timer 0. This pin operates as PPG00 when it is used in PPG0 output mode.	25	20	H1	15	H2
	RTO01_1 (PPG00_1)		85	-	-	-	-
	RTO02_0 (PPG02_0)	Waveform generator output pin of multi-function timer 0. This pin operates as PPG02 when it is used in PPG0 output mode.	26	21	H2	16	H3
	RTO02_1 (PPG02_1)		84	-	-	-	-
	RTO03_0 (PPG02_0)	Waveform generator output pin of multi-function timer 0. This pin operates as PPG02 when it is used in PPG0 output mode.	27	22	G4	17	J1
	RTO03_1 (PPG02_1)		83	-	-	-	-
	RTO04_0 (PPG04_0)	Waveform generator output pin of multi-function timer 0. This pin operates as PPG04 when it is used in PPG0 output mode.	28	23	H3	18	J2
	RTO04_1 (PPG04_1)		82	-	-	-	-
	RTO05_0 (PPG04_0)	Waveform generator output pin of multi-function timer 0. This pin operates as PPG04 when it is used in PPG0 output mode.	29	24	J2	19	J4
	RTO05_1 (PPG04_1)		81	-	-	-	-
	IGTRG_0	PPG IGMT mode external trigger input pin	46	41	L7	31	J6
	IGTRG_1		116	96	C4	76	C4

Pin Function	Pin Name	Function Description	Pin No				
			LQFP-120	LQFP-100	BGA-112	LQFP-80	BGA-96
Quadrature Position/ Revolution Counter 0	AIN0_0	QPRC ch.0 AIN input pin	14	9	E1	9	E2
	AIN0_1		45	40	J6	30	K6
	AIN0_2		2	2	C1	2	C1
	BIN0_0	QPRC ch.0 BIN input pin	15	10	E2	10	E3
	BIN0_1		46	41	L7	31	J6
	BIN0_2		3	3	C2	3	C2
	ZIN0_0	QPRC ch.0 ZIN input pin	16	11	E3	11	G1
	ZIN0_1		47	42	K7	32	L7
	ZIN0_2		4	4	B3	4	B3
Quadrature Position/ Revolution Counter 1	AIN1_1	QPRC ch.1 AIN input pin	89	74	C10	60	C10
	AIN1_2		48	43	H6	33	K7
	BIN1_1	QPRC ch.1 BIN input pin	88	73	C11	59	C11
	BIN1_2		49	44	J7	34	J7
	ZIN1_1	QPRC ch.1 ZIN input pin	87	72	E8	58	D9
	ZIN1_2		50	45	K8	35	K8
Real-time clock	RTCCO_0	0.5 seconds pulse output pin of Real-time clock	107	92	B5	72	A6
	RTCCO_1		65	55	H10	45	H10
	RTCCO_2		24	19	G3	14	H1
	SUBOUT_0	Sub clock output pin	107	92	B5	72	A6
	SUBOUT_1		65	55	H10	45	H10
	SUBOUT_2		24	19	G3	14	H1
Low-Power Consumption Mode	WKUP0	Deep standby mode return signal input pin 0	107	92	B5	72	A6
	WKUP1	Deep standby mode return signal input pin 1	63	53	J10	43	J10
	WKUP2	Deep standby mode return signal input pin 2	88	73	C11	59	C11
	WKUP3	Deep standby mode return signal input pin 3	116	96	C4	76	C4
	WKUP4	Deep standby mode return signal input pin 4	14	9	E1	9	E2
	WKUP5	Deep standby mode return signal input pin 5	102	87	D7	67	C8
HDMI-CEC/ Remote Control Reception	CEC0_0	HDMI-CEC/Remote Control Reception ch.0 input/output pin	48	43	H6	33	K7
	CEC0_1		103	88	A6	68	C7
	CEC1_0	HDMI-CEC/Remote Control Reception ch.1 input/output pin	116	96	C4	76	C4
	CEC1_1		8	8	D5	8	E1

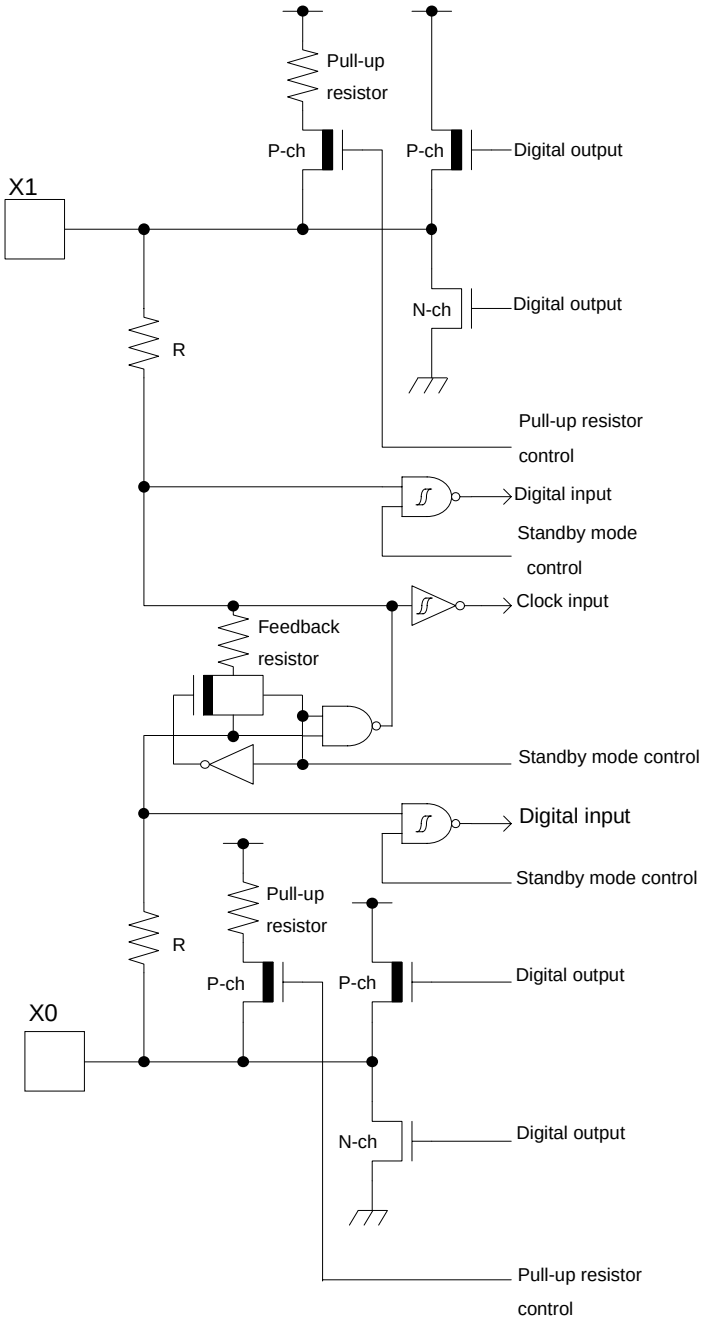
Pin function	Pin name	Function description	Pin No				
			LQFP-120	LQFP-100	BGA-112	LQFP-80	BGA-96
Reset	INITX	External Reset Input pin. A reset is valid when INITX=L.	43	38	K4	28	K4
Mode	MD0	Mode 0 pin. During normal operation, MD0=L must be input. During serial programming to Flash memory, MD0=H must be input.	57	47	L8	37	L8
	MD1	Mode 1 pin. During serial programming to Flash memory, MD1=L must be input.	56	46	K9	36	K9
Power	VCC	Power supply pin	1	1	B1	1	B1
	VCC	Power supply pin	31	26	J1	-	-
	VCC	Power supply pin	40	35	K1	25	K1
	VCC	Power supply pin	61	51	K11	41	K11
	VCC	Power supply pin	91	76	A10	-	-
	VCC	Power supply pin	117	97	A4	77	A4
GND	VSS	GND pin	-	-	-	-	F1
	VSS	GND pin	-	-	-	-	F2
	VSS	GND pin	-	-	-	-	F3
	VSS	GND pin	-	-	B2	-	B2
	VSS	GND pin	30	25	L1	20	L1
	VSS	GND pin	-	-	K2	-	K2
	VSS	GND pin	-	-	J3	-	J3
	VSS	GND pin	-	-	H4	-	-
	VSS	GND pin	-	-	-	-	L6
	VSS	GND pin	39	34	L4	24	L4
	VSS	GND pin	60	50	L11	40	L11
	VSS	GND pin	-	-	K10	-	K10
	VSS	GND pin	-	-	J9	-	J9
	VSS	GND pin	-	-	H8	-	-
	VSS	GND pin	-	-	B10	-	B10
	VSS	GND pin	-	-	C9	-	C9
	VSS	GND pin	-	-	-	-	D11
	VSS	GND pin	90	75	A11	-	A11
	VSS	GND pin	-	-	D8	-	-
	VSS	GND pin	-	-	-	-	A7
	VSS	GND pin	-	-	D4	-	-
	VSS	GND pin	-	-	C3	-	C3
	VSS	GND pin	-	-	-	-	A5
	VSS	GND pin	120	100	A1	80	A1

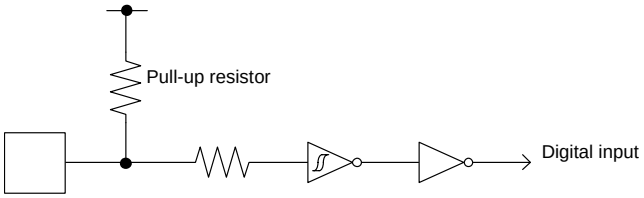
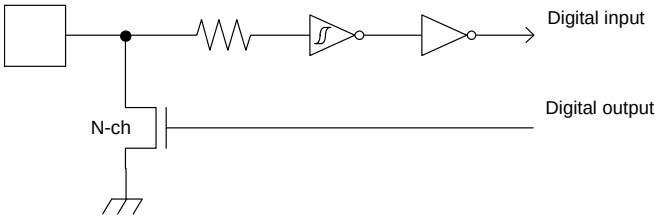
Pin Function	Pin Name	Function Description	Pin No				
			LQFP-120	LQFP-100	BGA-112	LQFP-80	BGA-96
Clock	X0	Main clock (oscillation) input pin	58	48	L9	38	L9
	X0A	Sub clock (oscillation) input pin	41	36	L3	26	L3
	X1	Main clock (oscillation) I/O pin	59	49	L10	39	L10
	X1A	Sub clock (oscillation) I/O pin	42	37	K3	27	K3
	CROUT_0	Built-in High-speed CR-osc clock output port	89	74	C10	60	C10
	CROUT_1		107	92	B5	72	A6
ADC Power	AVCC	A/D converter analog power supply pin	70	60	H11	50	H11
	AVRH	A/D converter analog reference voltage input pin	71	61	F11	51	F11
ADC GND	AVSS	A/D converter GND pin	72	62	G11	52	G11
C pin	C	Power stabilization capacity pin	38	33	L2	23	L2

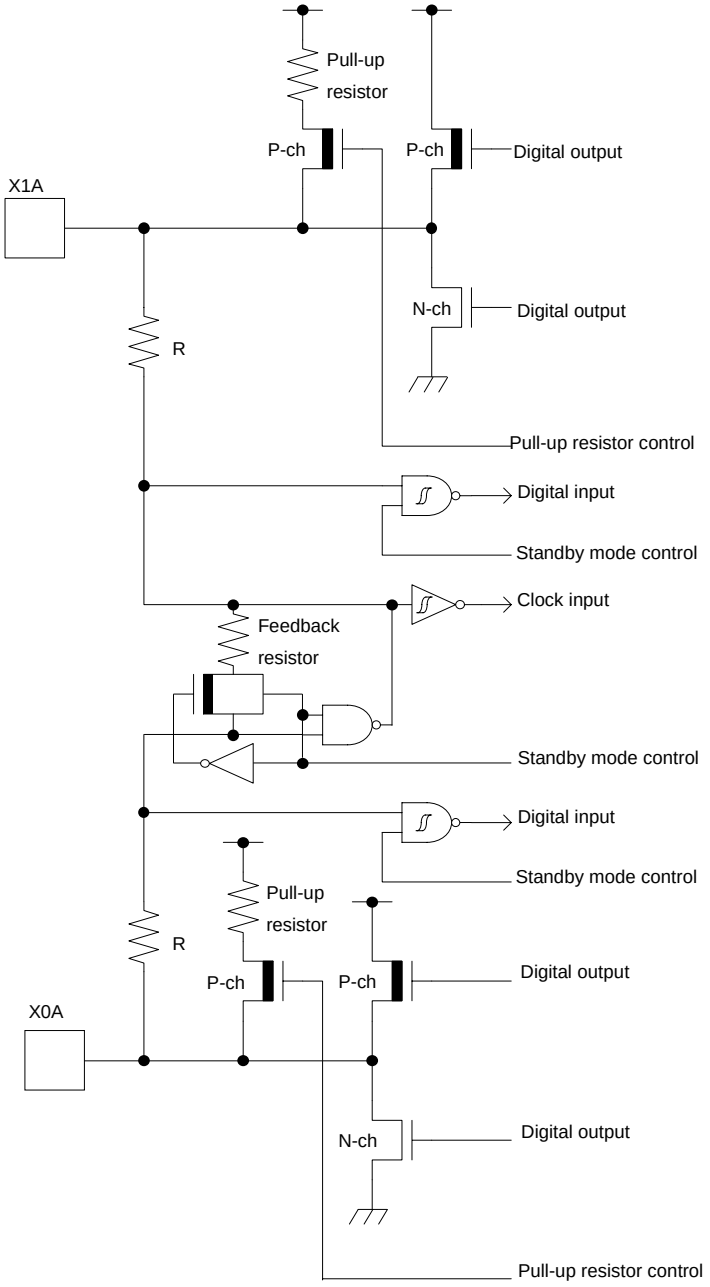
Note:

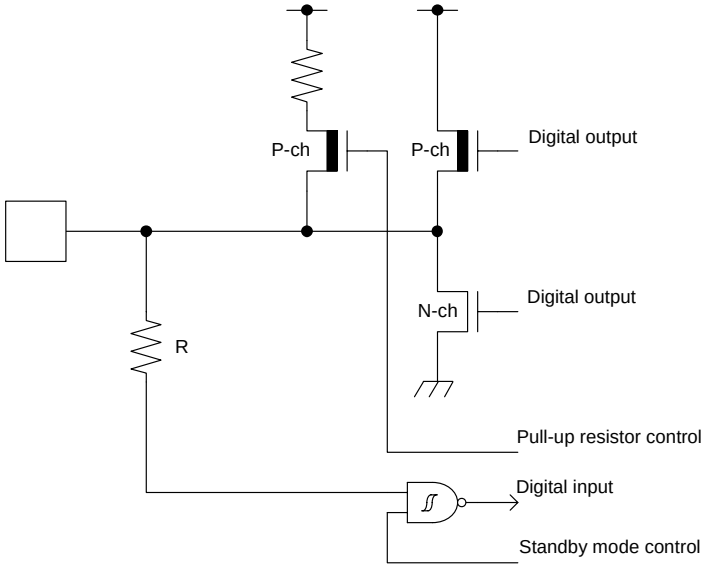
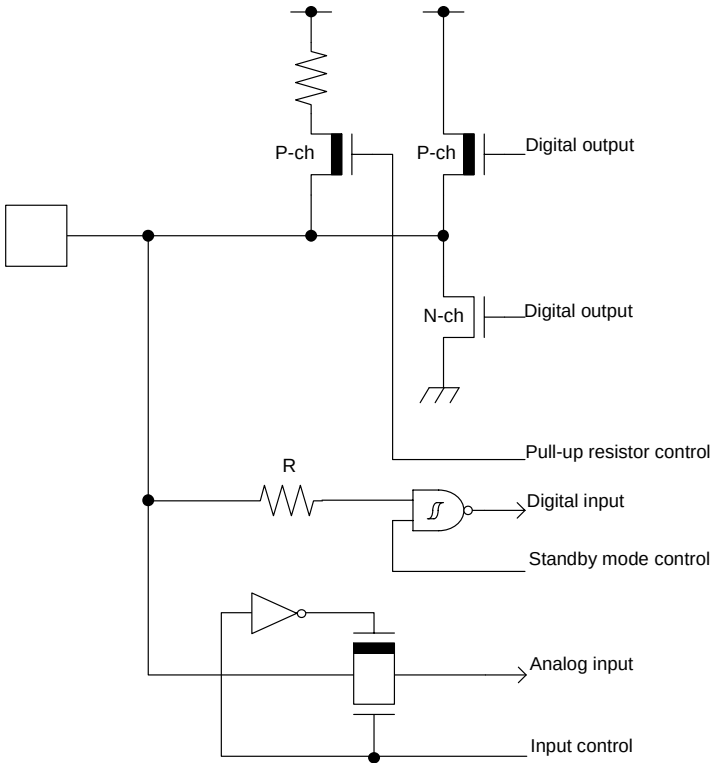
- *While this device contains a Test Access Port (TAP) based on the IEEE 1149.1-2001 JTAG standard, it is not fully compliant to all requirements of that standard. This device may contain a 32-bit device ID that is the same as the 32-bit device ID in other devices with different functionality. The TAP pins may also be configurable for purposes other than access to the TAP controller.*

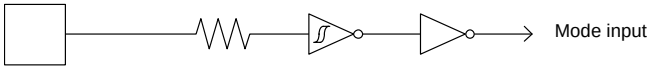
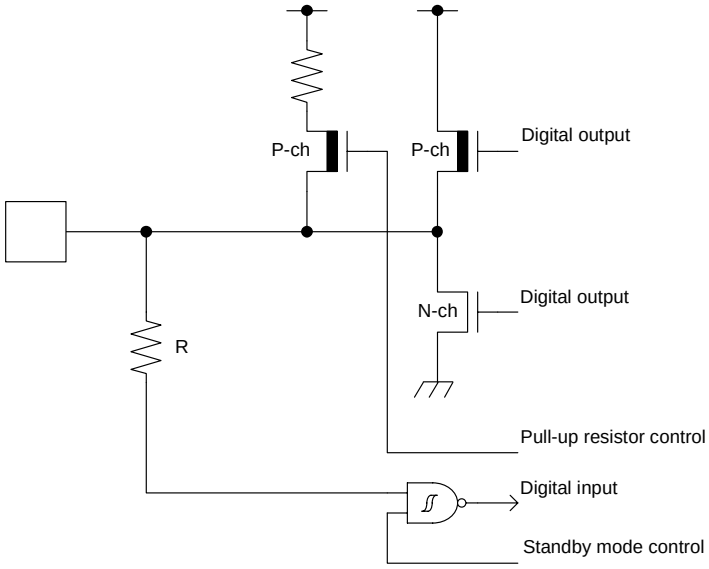
5. I/O Circuit Type

Type	Circuit	Remarks
A		It is possible to select the main oscillation / GPIO function When the main oscillation is selected. ■ Oscillation feedback resistor: Approximately 1 MΩ ■ With standby mode control When the GPIO is selected. ■ CMOS level output. ■ CMOS level hysteresis input ■ With pull-up resistor control ■ With standby mode control ■ Pull-up resistor: Approximately 33 kΩ ■ I_{OH}= -4 mA, I_{OL}= 4 mA

Type	Circuit	Remarks
B		■ CMOS level hysteresis input ■ Pull-up resistor: Approximately 33 kΩ
C		■ Open drain output ■ CMOS level hysteresis input

Type	Circuit	Remarks
D		It is possible to select the sub oscillation / GPIO function When the sub oscillation is selected. ■ Oscillation feedback resistor : Approximately 5MΩ ■ With standby mode control When the GPIO is selected. ■ CMOS level output. ■ CMOS level hysteresis input ■ With pull-up resistor control ■ With standby mode control ■ Pull-up resistor: Approximately 33 kΩ ■ I_{OH}= -4 mA, I_{OL}= 4 mA

Type	Circuit	Remarks
E		■ CMOS level output ■ CMOS level hysteresis input ■ With pull-up resistor control ■ With standby mode control ■ Pull-up resistor : Approximately 33 kΩ ■ I_{OH}= -4 mA, I_{OL}= 4 mA ■ When this pin is used as an I^2C pin, the digital output P-ch transistor is always off
F		■ CMOS level output ■ CMOS level hysteresis input ■ With input control ■ Analog input ■ With pull-up resistor control ■ With standby mode control ■ Pull-up resistor : Approximately 33 kΩ ■ I_{OH}= -4 mA, I_{OL}= 4 mA ■ When this pin is used as an I^2C pin, the digital output P-ch transistor is always off

Type	Circuit	Remarks
G		CMOS level hysteresis input
H		■ CMOS level output ■ CMOS level hysteresis input ■ 5 V tolerant ■ With pull-up resistor control ■ With standby mode control ■ Pull-up resistor: Approximately 33 kΩ ■ I_{OH}= -4 mA, I_{OL}= 4 mA ■ Available to control PZR registers. ■ When this pin is used as an I^2C pin, the digital output P-ch transistor is always off

6. Handling Precautions

Any semiconductor devices have inherently a certain rate of failure. The possibility of failure is greatly affected by the conditions in which they are used (circuit conditions, environmental conditions, etc.). This page describes precautions that must be observed to minimize the chance of failure and to obtain higher reliability from your Cypress semiconductor devices.

6.1 Precautions for Product Design

This section describes precautions when designing electronic equipment using semiconductor devices.

■ Absolute Maximum Ratings

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of certain established limits, called absolute maximum ratings. Do not exceed these ratings.

■ Recommended Operating Conditions

Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their sales representative beforehand.

■ Processing and Protection of Pins

These precautions must be followed when handling the pins which connect semiconductor devices to power supply and input/output functions.

1. Preventing Over-Voltage and Over-Current Conditions

Exposure to voltage or current levels in excess of maximum ratings at any pin is likely to cause deterioration within the device, and in extreme cases leads to permanent damage of the device. Try to prevent such overvoltage or over-current conditions at the design stage.

2. Protection of Output Pins

Shorting of output pins to supply pins or other output pins, or connection to large capacitance can cause large current flows. Such conditions if present for extended periods of time can damage the device. Therefore, avoid this type of connection.

3. Handling of Unused Input Pins

Unconnected input pins with very high impedance levels can adversely affect stability of operation. Such pins should be connected through an appropriate resistance to a power supply pin or ground pin.

■ Latch-up

Semiconductor devices are constructed by the formation of P-type and N-type areas on a substrate. When subjected to abnormally high voltages, internal parasitic PNPN junctions (called thyristor structures) may be formed, causing large current levels in excess of several hundred mA to flow continuously at the power supply pin. This condition is called latch-up.

CAUTION:

The occurrence of latch-up not only causes loss of reliability in the semiconductor device, but can cause injury or damage from high heat, smoke or flame. To prevent this from happening, do the following:

1. *Be sure that voltages applied to pins do not exceed the absolute maximum ratings. This should include attention to abnormal noise, surge levels, etc.*
2. *Be sure that abnormal current flows do not occur during the power-on sequence.*

■ Observance of Safety Regulations and Standards

Most countries in the world have established standards and regulations regarding safety, protection from electromagnetic interference, etc. Customers are requested to observe applicable regulations and standards in the design of products.

■ Fail-Safe Design

Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

■ Precautions Related to Usage of Devices

Cypress semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).

CAUTION:

Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

6.2 Precautions for Package Mounting

Package mounting may be either lead insertion type or surface mount type. In either case, for heat resistance during soldering, you should only mount under Cypress' recommended conditions. For detailed information about mount conditions, contact your sales representative.

■ Lead Insertion Type

Mounting of lead insertion type packages onto printed circuit boards may be done by two methods: direct soldering on the board, or mounting by using a socket.

Direct mounting onto boards normally involves processes for inserting leads into through-holes on the board and using the flow soldering (wave soldering) method of applying liquid solder. In this case, the soldering process usually causes leads to be subjected to thermal stress in excess of the absolute ratings for storage temperature. Mounting processes should conform to Cypress recommended mounting conditions.

If socket mounting is used, differences in surface treatment of the socket contacts and IC lead surfaces can lead to contact deterioration after long periods. For this reason it is recommended that the surface treatment of socket contacts and IC leads be verified before mounting.

■ Surface Mount Type

Surface mount packaging has longer and thinner leads than lead-insertion packaging, and therefore leads are more easily deformed or bent. The use of packages with higher pin counts and narrower pin pitch results in increased susceptibility to open connections caused by deformed pins, or shorting due to solder bridges.

You must use appropriate mounting techniques. Cypress recommends the solder reflow method, and has established a ranking of mounting conditions for each product. Users are advised to mount packages in accordance with Cypress ranking of recommended conditions.

■ Lead-Free Packaging

CAUTION:

When ball grid array (BGA) packages with Sn-Ag-Cu balls are mounted using Sn-Pb eutectic soldering, junction strength may be reduced under some conditions of use.

■ Storage of Semiconductor Devices

Because plastic chip packages are formed from plastic resins, exposure to natural environmental conditions will cause absorption of moisture. During mounting, the application of heat to a package that has absorbed moisture can cause surfaces to peel, reducing moisture resistance and causing packages to crack. To prevent, do the following:

1. Avoid exposure to rapid temperature changes, which cause moisture to condense inside the product. Store products in locations where temperature changes are slight.
2. Use dry boxes for product storage. Products should be stored below 70% relative humidity, and at temperatures between 5°C and 30°C. When you open Dry Package that recommends humidity 40% to 70% relative humidity.
3. When necessary, Cypress packages semiconductor devices in highly moisture-resistant aluminum laminate bags, with a silica gel desiccant. Devices should be sealed in their aluminum laminate bags for storage.
4. Avoid storing packages where they are exposed to corrosive gases or high levels of dust.

■ Baking

Packages that have absorbed moisture may be de-moisturized by baking (heat drying). Follow the Cypress recommended conditions for baking.

Condition: 125°C/24 h

■ Static Electricity

Because semiconductor devices are particularly susceptible to damage by static electricity, you must take the following precautions:

1. Maintain relative humidity in the working environment between 40% and 70%. Use of an apparatus for ion generation may be needed to remove electricity.
2. Electrically ground all conveyors, solder vessels, soldering irons and peripheral equipment.
3. Eliminate static body electricity by the use of rings or bracelets connected to ground through high resistance (on the level of 1 MΩ). Wearing of conductive clothing and shoes, use of conductive floor mats and other measures to minimize shock loads is recommended.
4. Ground all fixtures and instruments, or protect with anti-static measures.
5. Avoid the use of styrofoam or other highly static-prone materials for storage of completed board assemblies.

6.3 Precautions for Use Environment

Reliability of semiconductor devices depends on ambient temperature and other conditions as described above.

For reliable performance, do the following:

1. Humidity

Prolonged use in high humidity can lead to leakage in devices as well as printed circuit boards. If high humidity levels are anticipated, consider anti-humidity processing.

2. Discharge of Static Electricity

When high-voltage charges exist close to semiconductor devices, discharges can cause abnormal operation. In such cases, use anti-static measures or processing to prevent discharges.

3. Corrosive Gases, Dust, or Oil

Exposure to corrosive gases or contact with dust or oil may lead to chemical reactions that will adversely affect the device. If you use devices in such conditions, consider ways to prevent such exposure or to protect the devices.

4. Radiation, Including Cosmic Radiation

Most devices are not designed for environments involving exposure to radiation or cosmic radiation. Users should provide shielding as appropriate.

5. Smoke, Flame

CAUTION:

Plastic molded devices are flammable, and therefore should not be used near combustible substances. If devices begin to smoke or burn, there is danger of the release of toxic gases.

Customers considering the use of Cypress products in other special environmental conditions should consult with sales representatives.

7. Handling Devices

7.1 Power Supply Pins

In products with multiple VCC and VSS pins, respective pins at the same potential are interconnected within the device in order to prevent malfunctions such as latch-up. However, all of these pins should be connected externally to the power supply or ground lines in order to reduce electromagnetic emission levels, to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total output current rating.

Moreover, connect the current supply source with each Power supply pin and GND pin of this device at low impedance. It is also advisable that a ceramic capacitor of approximately 0.1 µF be connected as a bypass capacitor between each Power supply pin and GND pin, between AVCC pin and AVSS pin near this device.

7.2 Stabilizing Power Supply Voltage

A malfunction may occur when the power supply voltage fluctuates rapidly even though the fluctuation is within the recommended operating conditions of the VCC power supply voltage. As a rule, with voltage stabilization, suppress the voltage fluctuation so that the fluctuation in VCC ripple (peak-to-peak value) at the commercial frequency (50 Hz/60 Hz) does not exceed 10% of the VCC value in the recommended operating conditions, and the transient fluctuation rate does not exceed 0.1 V/µs when there is a momentary fluctuation on switching the power supply.

7.3 Crystal Oscillator Circuit

Noise near the X0/X1 and X0A/X1A pins may cause the device to malfunction. Design the printed circuit board so that X0/X1, X0A/X1A pins, the crystal oscillator, and the bypass capacitor to ground are located as close to the device as possible.

It is strongly recommended that the PC board artwork be designed such that the X0/X1 and X0A/X1A pins are surrounded by ground plane as this is expected to produce stable operation.

Evaluate oscillation of your using crystal oscillator by your mount board.

7.4 Sub Crystal Oscillator

This series sub oscillator circuit is low gain to keep the low current consumption.

The crystal oscillator to fill the following conditions is recommended for sub crystal oscillator to stabilize the oscillation.

- Surface mount type

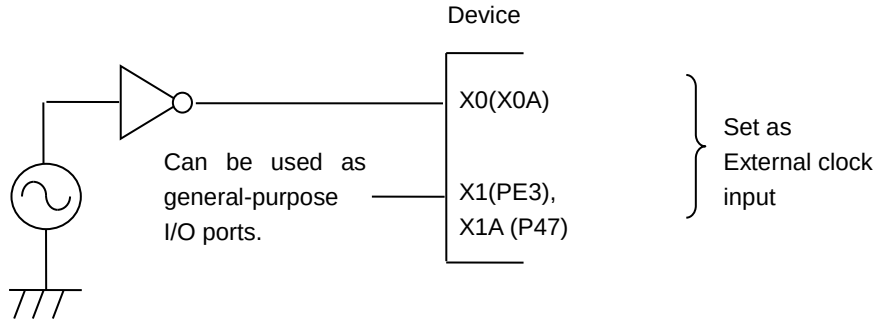
  Size : More than 3.2 mm × 1.5 mm
  Load capacitance : Approximately 6 pF to 7 pF
- Lead type

  Load capacitance : Approximately 6 pF to 7 pF

7.5 Using an external clock

When using an external clock as an input of the main clock, set X0/X1 to the external clock input, and input the clock to X0. X1(PE3) can be used as a general-purpose I/O port. Similarly, when using an external clock as an input of the sub clock, set X0A/X1A to the external clock input, and input the clock to X0A. X1A (P47) can be used as a general-purpose I/O port.

Example of Using an External Clock

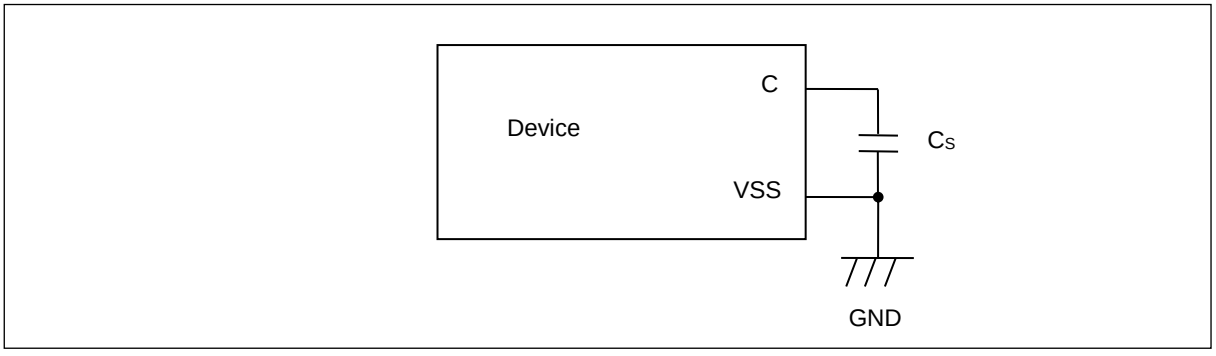


7.6 Handling when using Multi-function serial pin as I²C pin

If it is using the multi-function serial pin as I²C pins, P-ch transistor of digital output is always disabled. However, I²C pins need to keep the electrical characteristic like other pins and not to connect to the external I²C bus system with power OFF.

7.7 C pin

This series contains the regulator. Be sure to connect a smoothing capacitor (C_S) for the regulator between the C pin and the GND pin. Please use a ceramic capacitor or a capacitor of equivalent frequency characteristics as a smoothing capacitor. However, some laminated ceramic capacitors have the characteristics of capacitance variation due to thermal fluctuation (F characteristics and Y5V characteristics). Please select the capacitor that meets the specifications in the operating conditions to use by evaluating the temperature characteristics of a capacitor. A smoothing capacitor of about 4.7 µF would be recommended for this series.



7.8 Mode pins (MD0)

Connect the MD pin (MD0) directly to VCC or VSS pins. Design the printed circuit board such that the pull-up/down resistor stays low, as well as the distance between the mode pins and VCC pins or VSS pins is as short as possible and the connection impedance is low, when the pins are pulled-up/down such as for switching the pin level and rewriting the Flash memory data. It is because of preventing the device erroneously switching to test mode due to noise.

7.9 Notes on power-on

Turn power on/off in the following order or at the same time.
If not using the A/D converter, connect AVCC = VCC and AVSS = VSS.

Turning on : VCC →AVCC → AVRH

Turning off : AVRH → AVCC → VCC

7.10 Serial Communication

There is a possibility to receive wrong data due to the noise or other causes on the serial communication.

Therefore, design a printed circuit board so as to avoid noise.

Consider the case of receiving wrong data due to noise, perform error detection such as by applying a checksum of data at the end. If an error is detected, retransmit the data.

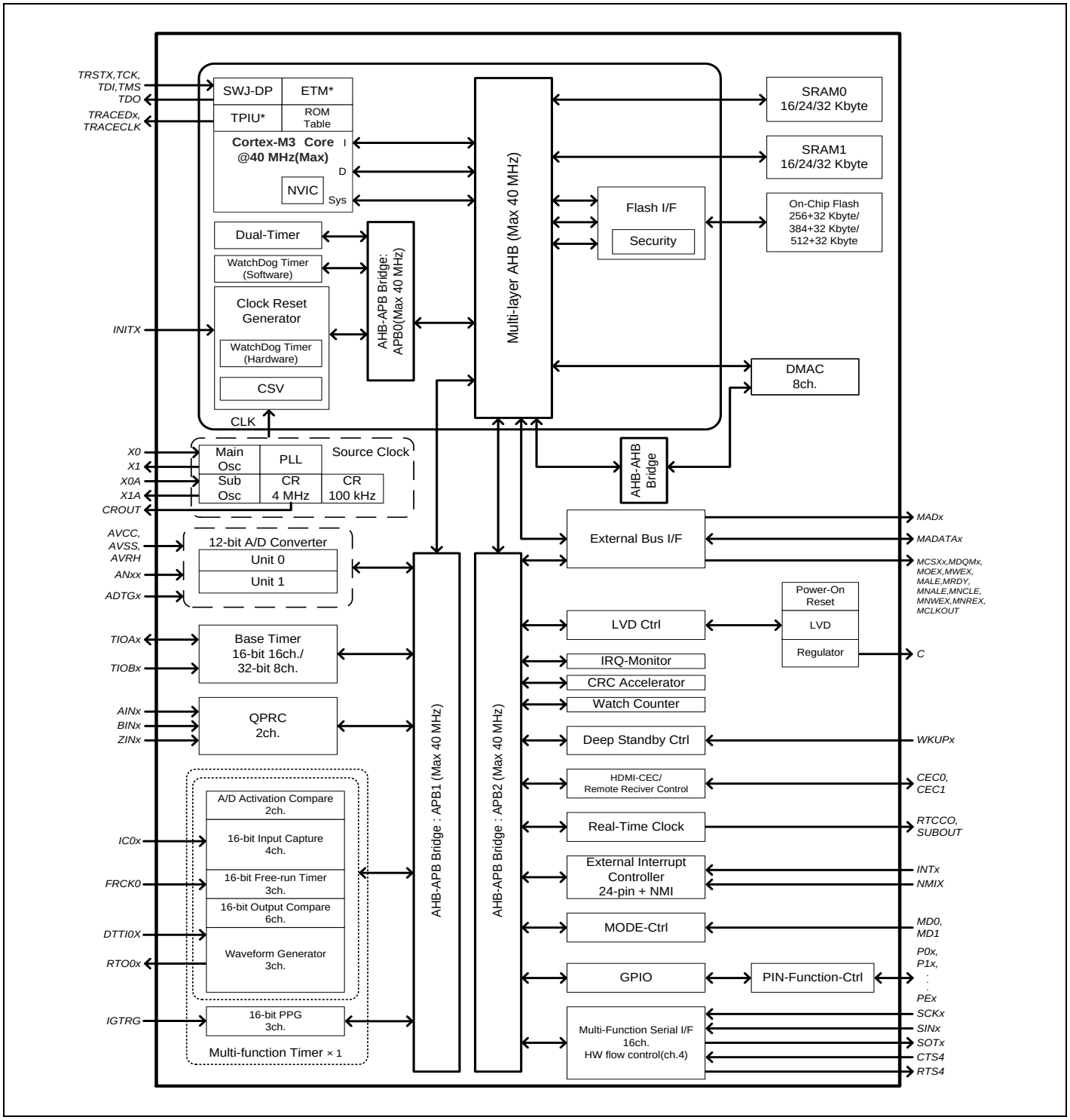
7.11 Differences in features among the products with different memory sizes and between Flash memory products and MASK products

The electric characteristics including power consumption, ESD, latch-up, noise characteristics, and oscillation characteristics among the products with different memory sizes and between Flash memory products and MASK products are different because chip layout and memory structures are different.
If you are switching to use a different product of the same series, please make sure to evaluate the electric characteristics.

7.12 Pull-Up function of 5 V tolerant I/O

Please do not input the signal more than VCC voltage at the time of Pull-Up function use of 5 V tolerant I/O.

8. Block Diagram



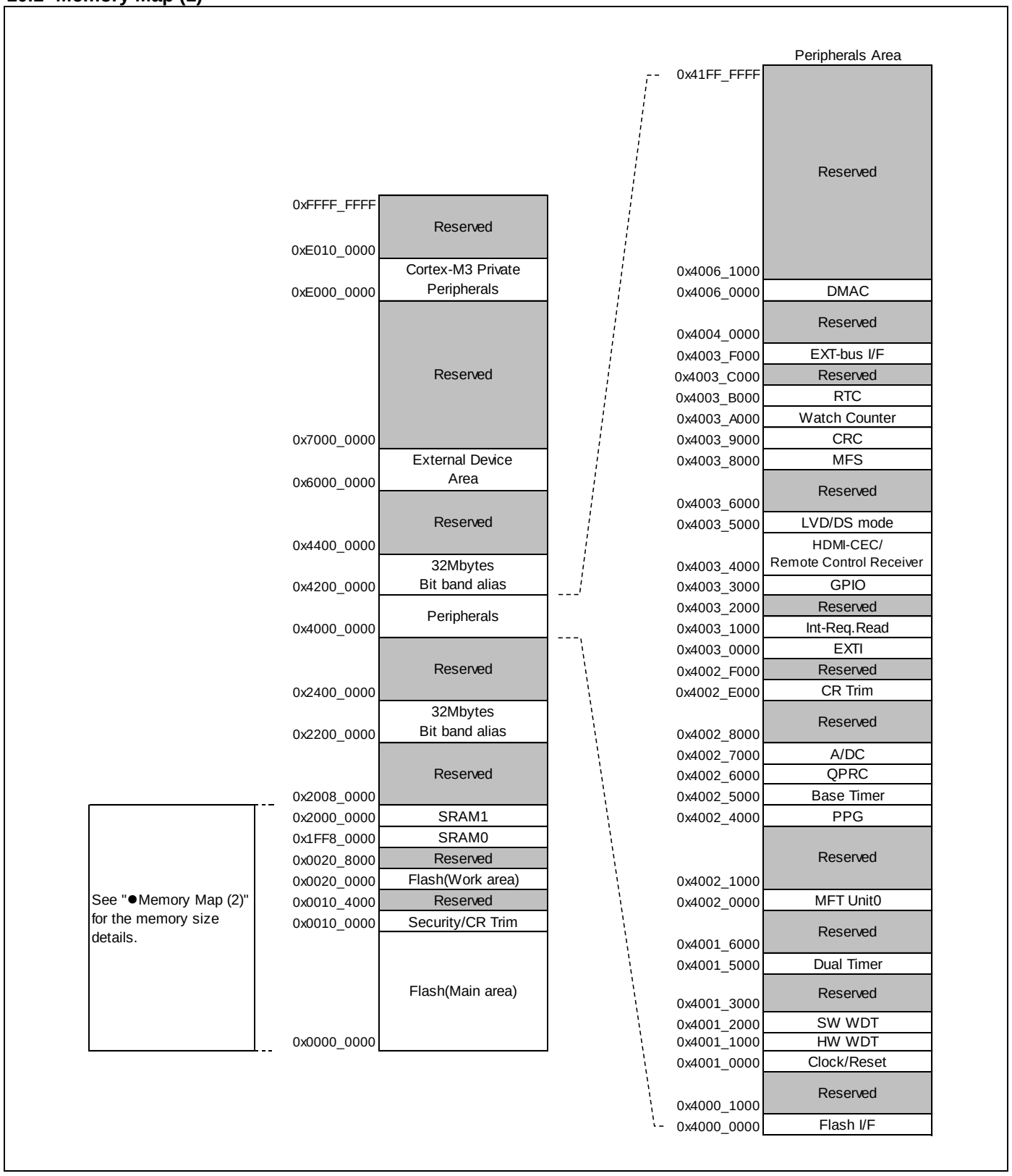
*:For the MB9AF154MB, MB9AF155MB, and MB9AF156MB, ETM is not available.

9. Memory Size

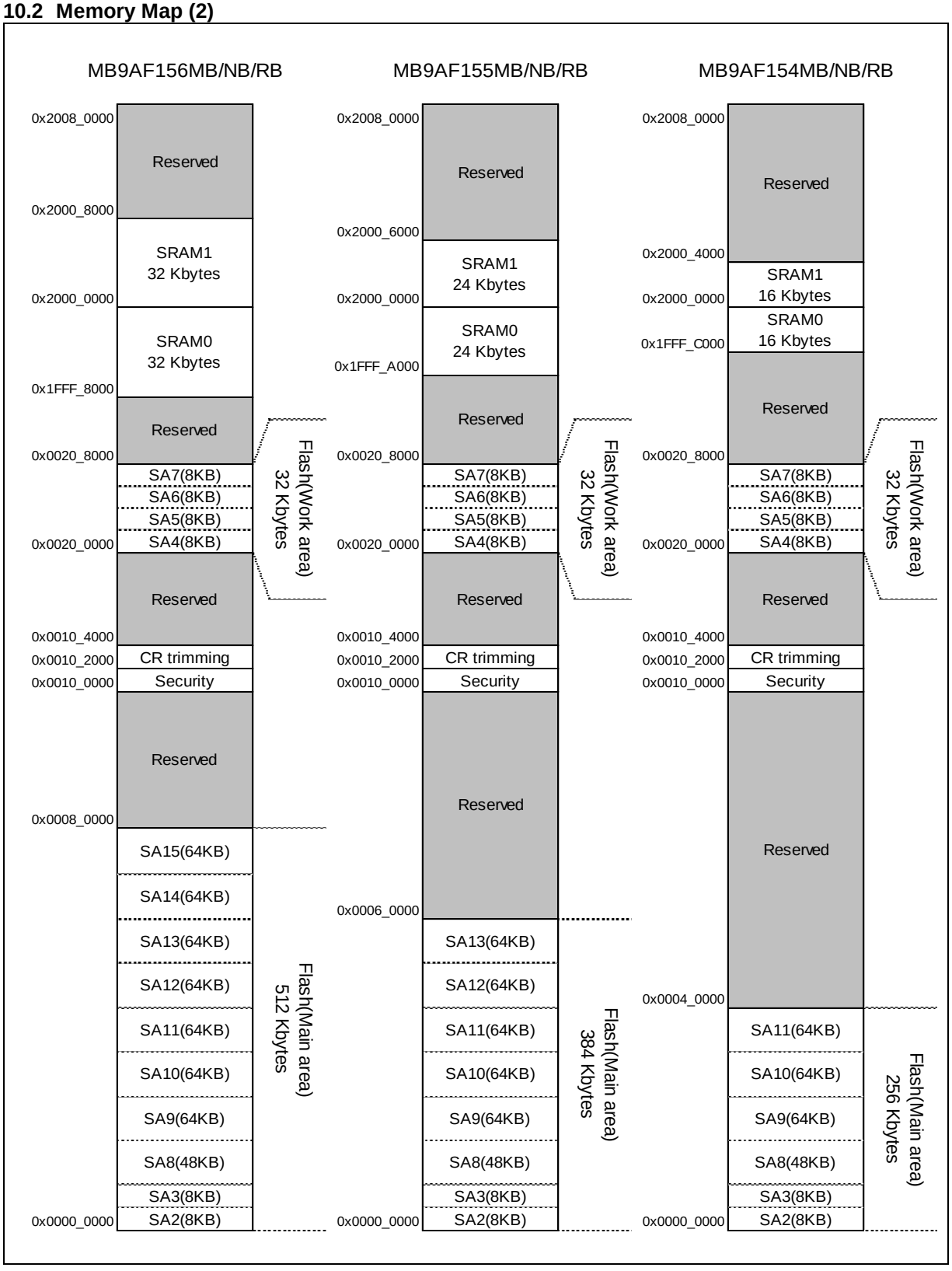
See Memory size in Product Lineup to confirm the memory size.

10. Memory Map

10.1 Memory Map (1)



10.2 Memory Map (2)



For more information about Flash (Main area)/Flash (Work area),

see MB9AB40N/A40N/340N/140N/150R, MB9B520M/320M/120M Series Flash Programming Manual.

10.3 Peripheral Address Map

Start address	End address	Bus	Peripherals
0x4000_0000	0x4000_0FFF	AHB	Flash memory I/F register
0x4000_1000	0x4000_FFFF		Reserved
0x4001_0000	0x4001_0FFF	APB0	Clock/Reset Control
0x4001_1000	0x4001_1FFF		Hardware Watchdog timer
0x4001_2000	0x4001_2FFF		Software Watchdog timer
0x4001_3000	0x4001_4FFF		Reserved
0x4001_5000	0x4001_5FFF		Dual Timer
0x4001_6000	0x4001_FFFF		Reserved
0x4002_0000	0x4002_0FFF	APB1	Multi-function timer unit0
0x4002_1000	0x4002_3FFF		Reserved
0x4002_4000	0x4002_4FFF		PPG
0x4002_5000	0x4002_5FFF		Base Timer
0x4002_6000	0x4002_6FFF		Quadrature Position/Revolution Counter
0x4002_7000	0x4002_7FFF		A/D Converter
0x4002_8000	0x4002_DFFF		Reserved
0x4002_E000	0x4002_EFFF		Built-in CR trimming
0x4002_F000	0x4002_FFFF		Reserved
0x4003_0000	0x4003_0FFF	APB2	External Interrupt
0x4003_1000	0x4003_1FFF		Interrupt Source Check Register
0x4003_2000	0x4003_2FFF		Reserved
0x4003_3000	0x4003_3FFF		GPIO
0x4003_4000	0x4003_4FFF		HDMI-CEC/Remote control Reception
0x4003_5000	0x4003_57FF		Low-Voltage Detector
0x4003_5800	0x4003_5FFF		Deep standby mode Controller
0x4003_6000	0x4003_7FFF		Reserved
0x4003_8000	0x4003_8FFF		Multi-function serial
0x4003_9000	0x4003_9FFF		CRC
0x4003_A000	0x4003_AFFF		Watch Counter
0x4003_B000	0x4003_BFFF		Real-time clock
0x4003_C000	0x4003_EFFF		Reserved
0x4003_F000	0x4003_FFFF		External bus interface
0x4004_0000	0x4005_FFFF	AHB	Reserved
0x4006_0000	0x4006_0FFF		DMAC register
0x4006_1000	0x41FF_FFFF		Reserved

11. Pin Status in Each CPU State

The terms used for pin status have the following meanings.

- INITX=0

This is the period when the INITX pin is the L level.

- INITX=1

This is the period when the INITX pin is the H level.

- SPL=0

This is the status that the standby pin level setting bit (SPL) in the standby mode control register (STB_CTL) is set to 0.

- SPL=1

This is the status that the standby pin level setting bit (SPL) in the standby mode control register (STB_CTL) is set to 1.

- Input enabled

Indicates that the input function can be used.

- Internal input fixed at 0

This is the status that the input function cannot be used. Internal input is fixed at L.

- Hi-Z

Indicates that the pin drive transistor is disabled and the pin is put in the Hi-Z state.

- Setting disabled

Indicates that the setting is disabled.

- Maintain previous state

Maintains the state that was immediately prior to entering the current mode.

If a built-in peripheral function is operating, the output follows the peripheral function.

If the pin is being used as a port, that output is maintained.

- Analog input is enabled

Indicates that the analog input is enabled.

- Trace output

Indicates that the trace function can be used.

- GPIO selected

In Deep standby mode, pins switch to the general-purpose I/O port.

11.1 List of Pin Status

Pin status type	Function group	Power-on reset or low-voltage detection state	INITX input state	Device internal reset state	Run mode or Sleep mode state	Timer mode, RTC mode, or Stop mode state		Deep standby Rtc mode or Deep standby Stop mode state		Return from Deep standby mode state
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable		Power supply stable		Power supply stable
		-	INITX = 0	INITX = 1	INITX = 1	INITX = 1		INITX = 1		INITX = 1
		-	-	-	-	SPL = 0	SPL = 1	SPL = 0	SPL = 1	-
A	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at 0	GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected
	Main crystal oscillator input pin/ External main clock input selected	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
B	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at 0	GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected
	External main clock input selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at 0	Maintain previous state	Hi-Z / Internal input fixed at 0	Maintain previous state
	Main crystal oscillator output pin	Hi-Z / Internal input fixed at 0/ or Input enable	Hi-Z / Internal input fixed at 0	Hi-Z / Internal input fixed at 0	Maintain previous state/ When oscillation stops[1], Hi-Z / Internal input fixed at 0	Maintain previous state/ When oscillation stops[1], Hi-Z / Internal input fixed at 0	Maintain previous state/ When oscillation stops[1], Hi-Z / Internal input fixed at 0	Maintain previous state/ When oscillation stops[1], Hi-Z / Internal input fixed at 0	Maintain previous state/ When oscillation stops[1], Hi-Z / Internal input fixed at 0	Maintain previous state/ When oscillation stops[1], Hi-Z / Internal input fixed at 0
C	INITX input pin	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled

Pin status type	Function group	Power-on reset or low-voltage detection state	INITX input state	Device internal reset state	Run mode or Sleep mode state	Timer mode, RTC mode, or Stop mode state		Deep standby Rtc mode or Deep standby Stop mode state		Return from Deep standby mode state
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable		Power supply stable		Power supply stable
		-	INITX = 0	INITX = 1	INITX = 1	INITX = 1		INITX = 1		INITX = 1
		-	-	-	-	SPL = 0	SPL = 1	SPL = 0	SPL = 1	-
D	Mode input pin	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
E	Mode input pin	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Input enabled	GPIO selected	Hi-Z / Input enabled	GPIO selected
F	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at 0	GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected
	Sub crystal oscillator input pin / External sub clock input selected	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled

Pin status type	Function group	Power-on reset or low-voltage detection state	INITX input state	Device internal reset state	Run mode or Sleep mode state	Timer mode, RTC mode, or Stop mode state		Deep standby Rtc mode or Deep standby Stop mode state		Return from Deep standby mode state
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable		Power supply stable		Power supply stable
		-	INITX = 0	INITX = 1	INITX = 1	INITX = 1		INITX = 1		INITX = 1
		-	-	-	-	SPL = 0	SPL = 1	SPL = 0	SPL = 1	-
G	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at 0	GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected
	External sub clock input selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at 0	Maintain previous state	Hi-Z/ Internal input fixed at 0	Maintain previous state
	Sub crystal oscillator output pin	Hi-Z / Internal input fixed at 0/ or Input enable	Hi-Z / Internal input fixed at 0	Hi-Z / Internal input fixed at 0	Maintain previous state	Maintain previous state/When oscillation stops[2], Hi-Z / Internal input fixed at 0	Maintain previous state/ When oscillation stops[2], Hi-Z / Internal input fixed at 0	Maintain previous state/ When oscillation stops[2], Hi-Z/ Internal input fixed at 0	Maintain previous state/When oscillation stops[2], Hi-Z/ Internal input fixed at 0	Maintain previous state/ When oscillation stops[2], Hi-Z/ Internal input fixed at 0
H	NMIX selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	WKUP input enabled	Hi-Z / WKUP input enabled	GPIO selected
	Resource other than above selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled			Hi-Z / Internal input fixed at 0			
	GPIO selected									

Pin status type	Function group	Power-on reset or low-voltage detection state	INITX input state	Device internal reset state	Run mode or Sleep mode state	Timer mode, RTC mode, or Stop mode state		Deep standby Rtc mode or Deep standby Stop mode state		Return from Deep standby mode state
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable		Power supply stable		Power supply stable
		-	INITX = 0	INITX = 1	INITX = 1	INITX = 1		INITX = 1		INITX = 1
		-	-	-	-	SPL = 0	SPL = 1	SPL = 0	SPL = 1	-
I	JTAG selected	Hi-Z	Pull-up / Input enabled	Pull-up / Input enabled	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state
	Resource selected	Setting disabled	Setting disabled	Setting disabled			Hi-Z / Internal input fixed at 0	GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected
	GPIO selected									
J	Resource selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at 0	GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected
	GPIO selected									
K	External interrupt enabled selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected
	Resource other than above selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled			Hi-Z / Internal input fixed at 0			
	GPIO selected									

Pin status type	Function group	Power-on reset or low-voltage detection state	INITX input state	Device internal reset state	Run mode or Sleep mode state	Timer mode, RTC mode, or Stop mode state		Deep standby Rtc mode or Deep standby Stop mode state		Return from Deep standby mode state
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable		Power supply stable		Power supply stable
		-	INITX = 0	INITX = 1	INITX = 1	INITX = 1		INITX = 1		INITX = 1
		-	-	-	-	SPL = 0	SPL = 1	SPL = 0	SPL = 1	-
L	Analog input selected	Hi-Z	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled
	Resource other than above selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at 0	GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected
	GPIO selected									
M	Analog input selected	Hi-Z	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled
	External interrupt enabled selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected
	Resource other than above selected						Hi-Z / Internal input fixed at 0			
	GPIO selected									

Pin status type	Function group	Power-on reset or low-voltage detection state	INITX input state	Device internal reset state	Run mode or Sleep mode state	Timer mode, RTC mode, or Stop mode state		Deep standby Rtc mode or Deep standby Stop mode state		Return from Deep standby mode state
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable		Power supply stable		Power supply stable
		-	INITX = 0	INITX = 1	INITX = 1	INITX = 1		INITX = 1		INITX = 1
		-	-	-	-	SPL = 0	SPL = 1	SPL = 0	SPL = 1	-
N	Analog input selected	Hi-Z	Hi-Z / Internal input fixed at 0 /Analog input enabled	Hi-Z / Internal input fixed at 0 /Analog input enabled	Hi-Z / Internal input fixed at 0 /Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 /Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 /Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled
	Trace selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Trace output	GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected
	Resource other than above selected						Hi-Z / Internal input fixed at 0			
	GPIO selected									
O	Analog input selected	Hi-Z	Hi-Z / Internal input fixed at 0 /Analog input enabled	Hi-Z / Internal input fixed at 0 /Analog input enabled	Hi-Z / Internal input fixed at 0 /Analog input enabled	Hi-Z / Internal input fixed at 0 /Analog input enabled	Hi-Z / Internal input fixed at 0 /Analog input enabled	Hi-Z / Internal input fixed at 0 /Analog input enabled	Hi-Z / Internal input fixed at 0 /Analog input enabled	Hi-Z / Internal input fixed at 0 /Analog input enabled
	Trace selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Trace output	GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected
	External interrupt enabled selected						Maintain previous state			
	Resource other than above selected						Hi-Z / Internal input fixed at 0			
	GPIO selected									

Pin status type	Function group	Power-on reset or low-voltage detection state	INITX input state	Device internal reset state	Run mode or Sleep mode state	Timer mode, RTC mode, or Stop mode state		Deep standby Rtc mode or Deep standby Stop mode state		Return from Deep standby mode state
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable		Power supply stable		Power supply stable
		-	INITX = 0	INITX = 1	INITX = 1	INITX = 1		INITX = 1		INITX = 1
		-	-	-	-	SPL = 0	SPL = 1	SPL = 0	SPL = 1	-
P	Analog input selected	Hi-Z	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled
	WKUP enabled	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	WKUP input enabled	Hi-Z / WKUP input enabled	GPIO selected
	External interrupt enabled selected							GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	
	Resource other than above selected						Hi-Z / Internal input fixed at 0			
	GPIO selected									

Pin status type	Function group	Power-on reset or low-voltage detection state	INITX input state	Device internal reset state	Run mode or Sleep mode state	Timer mode, RTC mode, or Stop mode state		Deep standby Rtc mode or Deep standby Stop mode state		Return from Deep standby mode state
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable		Power supply stable		Power supply stable
		-	INITX = 0	INITX = 1	INITX = 1	INITX = 1		INITX = 1		INITX = 1
		-	-	-	-	SPL = 0	SPL = 1	SPL = 0	SPL = 1	-
Q	CEC enabled	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state
	WKUP enabled	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	WKUP input enabled	Hi-Z / WKUP input enabled	GPIO selected
	External interrupt enabled selected							GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	
	Resource other than above selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled			Hi-Z / Internal input fixed at 0			
	GPIO selected									
R	CEC enabled	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state
	External interrupt enabled selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected
	Resource other than above selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled			Hi-Z / Internal input fixed at 0			
	GPIO selected									

Pin status type	Function group	Power-on reset or low-voltage detection state	INITX input state	Device internal reset state	Run mode or Sleep mode state	Timer mode, RTC mode, or Stop mode state		Deep standby Rtc mode or Deep standby Stop mode state		Return from Deep standby mode state
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable		Power supply stable		Power supply stable
		-	INITX = 0	INITX = 1	INITX = 1	INITX = 1		INITX = 1		INITX = 1
		-	-	-	-	SPL = 0	SPL = 1	SPL = 0	SPL = 1	-
S	WKUP enabled	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	WKUP input enabled	Hi-Z / WKUP input enabled	GPIO selected
	External interrupt enabled selected							GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	
	Resource other than above selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled			Hi-Z / Internal input fixed at 0			
	GPIO selected									

[1]. Oscillation is stopped at Sub Timer mode, Low-speed CR Timer mode, RTC mode, Stop mode, Deep Standby RTC mode, and Deep Standby Stop mode.

[2]. Oscillation is stopped at Stop mode and Deep Standby Stop mode.

12. Electrical Characteristics

12.1 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage[1, 2]	V_{CC}	V_{SS} - 0.5	V_{SS} + 4.6	V	
Analog power supply voltage[1, 3]	AV_{CC}	V_{SS} - 0.5	V_{SS} + 4.6	V	
Analog reference voltage[1, 3]	AVRH	V_{SS} - 0.5	V_{SS} + 4.6	V	
Input voltage[1]	V_I	V_{SS} - 0.5	V_{CC} + 0.5 (≤ 4.6 V)	V	
		V_{SS} - 0.5	V_{SS} + 6.5	V	5 V tolerant
Analog pin input voltage[1]	V_{IA}	V_{SS} - 0.5	AV_{CC} + 0.5 (≤ 4.6 V)	V	
Output voltage[1]	V_O	V_{SS} - 0.5	V_{CC} + 0.5 (≤ 4.6 V)	V	
L level maximum output current[4]	I_{OL}	-	10	mA	
L level average output current[5]	I_{OLAV}	-	4	mA	
L level total maximum output current	$\sum I_{OL}$	-	100	mA	
L level total average output current[6]	$\sum I_{OLAV}$	-	50	mA	
H level maximum output current[4]	I_{OH}	-	- 10	mA	
H level average output current[5]	I_{OHAV}	-	- 4	mA	
H level total maximum output current	$\sum I_{OH}$	-	- 100	mA	
H level total average output current[6]	$\sum I_{OHAV}$	-	- 50	mA	
Power consumption	P_D	-	300	mW	
Storage temperature	T_{STG}	- 55	+ 150	°C	

[1]. These parameters are based on the condition that $V_{SS} = AV_{SS} = 0.0$ V.

[2]. V_{CC} must not drop below V_{SS} - 0.5 V.

[3]. Ensure that the voltage does not exceed V_{CC} + 0.5 V, for example, when the power is turned on.

[4]. The maximum output current is defined as the value of the peak current flowing through any one of the corresponding pins.

[5]. The average output current is defined as the average current value flowing through any one of the corresponding pins for a 100 ms period.

[6]. The total average output current is defined as the average current value flowing through all of corresponding pins for a 100 ms.

WARNING:

Semiconductor devices may be permanently damaged by application of stress (including, without limitation, voltage, current or temperature) in excess of absolute maximum ratings.Do not exceed any of these ratings.

12.2 Recommended Operating Conditions

(V_{SS} = AV_{SS} = 0.0V)

Parameter	Symbol	Conditions	Value		Unit	Remarks
			Min	Max		
Power supply voltage	V_{CC}	-	1.65[2]	3.6	V	
Analog power supply voltage	AV_{CC}	-	1.65	3.6	V	AV_{CC} = V_{CC}
Analog reference voltage	AVRH	-	2.7	AV_{CC}	V	AV_{CC} ≥ 2.7 V
			AV_{CC}	AV_{CC}	V	AV_{CC} < 2.7 V
Smoothing capacitor	C_S	-	1	10	µF	For built-in Regulator[1]
Operating temperature	T_A	-	- 40	+ 85	°C	

[1]. See C pin in Handling Devices for the connection of the smoothing capacitor.

[2]. In between less than the minimum power supply voltage and low voltage reset/interrupt detection voltage or more, instruction execution and low voltage detection function by built-in High-speed CR(including Main PLL is used) or built-in Low-speed CR is possible to operate only.

WARNING:

The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated under these conditions.

Any use of semiconductor devices will be under their recommended operating condition.

Operation under any conditions other than these conditions may adversely affect reliability of device and could result in device failure. No warranty is made with respect to any use, operating conditions or combinations not represented on this data sheet. If you are considering application under any conditions other than listed herein, please contact sales representatives beforehand.

12.3 DC Characteristics

12.3.1 *Current rating*

(V_{CC} = AV_{CC} = 1.65V to 3.6V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions		Value		Unit	Remarks
					Typ[3]	Max[4]		
Power supply current	I_{CC}	VCC	PLL Run mode	CPU: 40 MHz, Peripheral: 40 MHz	17.5	23.7	mA	[1], [5]
				CPU: 40 MHz, Peripheral: the clock stops NOP operation	8	11	mA	[1], [5]
			High-speed CR Run mode	CPU/ Peripheral: 4 MHz[2]	1.9	3.1	mA	[1]
			Sub Run mode	CPU/ Peripheral: 32 kHz	120	810	µA	[1], [6]
			Low-speed CR Run mode	CPU/ Peripheral: 100 kHz	140	830	µA	[1]
	I_{CCS}		PLL Sleep mode	Peripheral: 40 MHz	11	15	mA	[1], [5]
			High-speed CR Sleep mode	Peripheral: 4 MHz[2]	0.82	1.7	mA	[1]
			Sub Sleep mode	Peripheral: 32 kHz	105	800	µA	[1], [6]
			Low-speed CR Sleep mode	Peripheral: 100 kHz	125	810	µA	[1]

[1]. When all ports are fixed.

[2]. When setting it to 4 MHz by trimming.

[3]. T_A=+25°C, V_{CC}=3.6 V

[4]. T_A=+85°C, V_{CC}=3.6 V

[5]. When using the crystal oscillator of 4 MHz(Including the current consumption of the oscillation circuit)

[6]. When using the crystal oscillator of 32 kHz(Including the current consumption of the oscillation circuit)

Parameter	Symbol	Pin name	Conditions		Value		Unit	Remarks
					Typ[2]	Max[2]		
Power supply current	I_{CCT}	VCC	Main Timer mode	T_A = + 25°C, When LVD is off	2.0	2.7	mA	[1], [3]
				T_A = + 85°C, When LVD is off	-	3.2	mA	[1], [3]
			Sub Timer mode	T_A = + 25°C, When LVD is off	15	45	µA	[1], [4]
				T_A = + 85°C, When LVD is off	-	440	µA	[1], [4]
	I_{CCR}		RTC mode	T_A = + 25°C, When LVD is off	13	40	µA	[1], [4]
				T_A = + 85°C, When LVD is off	-	380	µA	[1], [4]
	I_{CCH}		Stop mode	T_A = + 25°C, When LVD is off	11	38	µA	[1]
				T_A = + 85°C, When LVD is off	-	370	µA	[1]
	I_{CCRD}		Deep Standby RTC mode	T_A = + 25°C, When LVD is off, When RAM is off	2.0	12	µA	[1], [4],[5]
				T_A = + 25°C, When LVD is off, When RAM is on	9.2	25	µA	[1], [4],[5]
				T_A = + 85°C, When LVD is off, When RAM is off	-	125	µA	[1], [4],[5]
				T_A = + 85°C, When LVD is off, When RAM is on		195	µA	[1], [4],[5]
	I_{CCHD}		Deep Standby Stop mode	T_A = + 25°C, When LVD is off, When RAM is off	1.4	10	µA	[1], [5]
				T_A = + 25°C, When LVD is off, When RAM is on	8.6	23	µA	[1], [5]
				T_A = + 85°C, When LVD is off, When RAM is off	-	120	µA	[1], [5]
				T_A = + 85°C, When LVD is off, When RAM is on		190	µA	[1], [5]

[1]. When all ports are fixed.

[2]. V_{CC}=3.6 V

[3]. When using the crystal oscillator of 4 MHz(Including the current consumption of the oscillation circuit)

[4]. When using the crystal oscillator of 32 kHz(Including the current consumption of the oscillation circuit)

[5]. RAM on/off setting is on-chip SRAM only.

12.3.1.1 Low-Voltage Detection Current

(V_{CC} = 1.65V to 3.6V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Typ	Max		
Low-voltage detection circuit (LVD) power supply current	I_{CCLVD}	VCC	At operation for reset V_{CC} = 3.6 V	0.13	0.3	µA	At not detect
			At operation for interrupt V_{CC} = 3.6 V	0.13	0.3	µA	At not detect

12.3.1.2 Flash Memory Current

(V_{CC} = 1.65V to 3.6V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Typ	Max		
Flash memory write/erase current	$I_{CCFLASH}$	VCC	At Write/Erase	9.5	11.2	mA	[1]

[1]. The current at which to write or erase Flash memory, $I_{CCFLASH}$ is added to I_{CC}.

12.3.1.3 A/D Converter Current

(V_{CC} = AV_{CC} = 1.65V to 3.6V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to +85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Typ	Max		
Power supply current	I_{CCAD}	AVCC	At 1unit operation	0.27	0.42	mA	
			At stop	0.03	10	µA	
Reference power supply current	I_{CCAVRH}	AVRH	At 1unit operation AVRH=3.6 V	0.72	1.29	mA	
			At stop	0.02	2.6	µA	

12.3.2 *Pin Characteristics*

(V_{CC} = AV_{CC} = 1.65V to 3.6V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
H level input Voltage (hysteresis input)	V_{IHS}	CMOS hysteresis input pin, MD0, MD1	$V_{CC} \geq 2.7$ V	$V_{CC} \times 0.8$	-	$V_{CC} + 0.3$	V	
			$V_{CC} < 2.7$ V	$V_{CC} \times 0.7$				
		5V tolerant input pin	$V_{CC} \geq 2.7$ V	$V_{CC} \times 0.8$	-	$V_{SS} + 5.5$	V	
			$V_{CC} < 2.7$ V	$V_{CC} \times 0.7$				
L level input Voltage (hysteresis input)	V_{ILS}	CMOS hysteresis input pin, MD0, MD1	$V_{CC} \geq 2.7$ V	V_{SS} - 0.3	-	$V_{CC} \times 0.2$	V	
			$V_{CC} < 2.7$ V			$V_{CC} \times 0.3$		
		5 V tolerant input pin	$V_{CC} \geq 2.7$ V	V_{SS} - 0.3	-	$V_{CC} \times 0.2$	V	
			$V_{CC} < 2.7$ V			$V_{CC} \times 0.3$		
H level output voltage	V_{OH}	4mA type	$V_{CC} \geq 2.7$ V, I_{OH} = - 4 mA	V_{CC} - 0.5	-	V_{CC}	V	
			$V_{CC} < 2.7$ V, I_{OH} = - 2 mA	V_{CC} - 0.45				
L level output voltage	V_{OL}	4mA type	$V_{CC} \geq 2.7$ V, I_{OL} = 4 mA	V_{SS}	-	0.4	V	
			$V_{CC} < 2.7$ V, I_{OL} = 2 mA					
Input leak current	I_{IL}	-	-	- 5	-	+ 5	µA	
		CEC0_0, CEC0_1, CEC1_0, CEC1_1	V_{CC} = AV_{CC} = AVRH = V_{SS} = AV_{SS} = 0.0 V	-	-	+1.8	µA	
Pull-up resistor value	R_{PU}	Pull-up pin	$V_{CC} \geq 2.7$ V	21	33	66	kΩ	
			$V_{CC} < 2.7$ V	-	-	134		
Input capacitance	C_{IN}	Other than VCC, VSS, AVCC, AVSS, AVRH	-	-	5	15	pF	

12.4 AC Characteristics

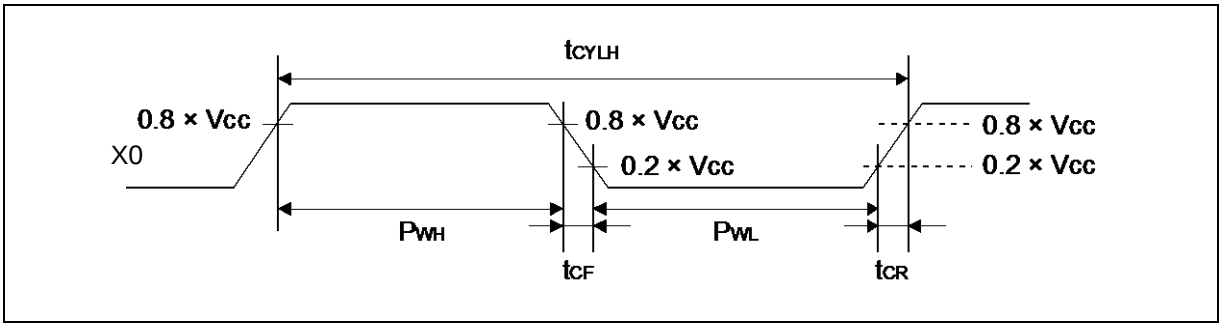
12.4.1 *Main Clock Input Characteristics*

(V_{CC} = 1.65V to 3.6V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input frequency	f_{CH}	X0, X1	$V_{CC} \geq 2.7V$	4	48	MHz	When crystal oscillator is connected
			$V_{CC} < 2.7V$	4	20		
			-	4	48	MHz	When using external clock
Input clock cycle	t_{CYLH}		-	20.83	250	ns	When using external clock
Input clock pulse width	-		PWH/tCYLH, PWL/tCYLH	45	55	%	When using external clock
Input clock rising time and falling time	t_{CF}, t_{CR}		-	-	5	ns	When using external clock
Internal operating clock[1] frequency	f_{CM}	-	-	-	40	MHz	Master clock
	f_{CC}	-	-	-	40	MHz	Base clock (HCLK/FCLK)
	f_{CP0}	-	-	-	40	MHz	APB0 bus clock[2]
	f_{CP1}	-	-	-	40	MHz	APB1 bus clock[2]
	f_{CP2}	-	-	-	40	MHz	APB2 bus clock[2]
Internal operating clock[1] cycle time	t_{CYCC}	-	-	25	-	ns	Base clock (HCLK/FCLK)
	t_{CYCP0}	-	-	25	-	ns	APB0 bus clock[2]
	t_{CYCP1}	-	-	25	-	ns	APB1 bus clock[2]
	t_{CYCP2}	-	-	25	-	ns	APB2 bus clock[2]

[1]. For more information about each internal operating clock, see Chapter 2-1: Clock in FM3 Family Peripheral Manual.

[2]. For about each APB bus which each peripheral is connected to, see Block Diagram in this data sheet.

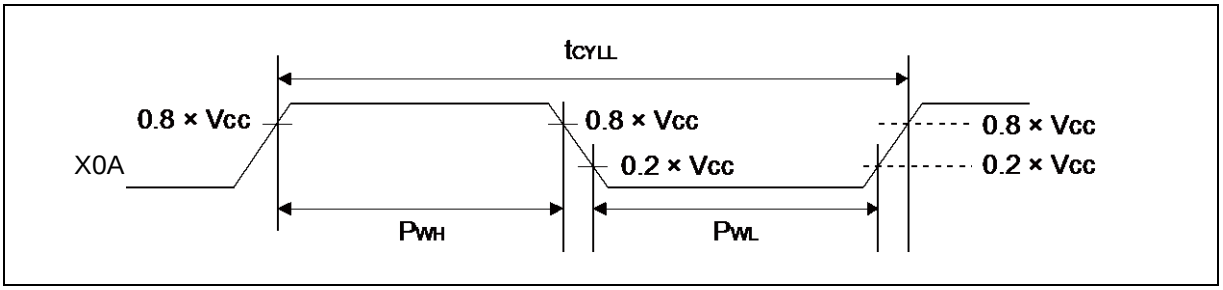


12.4.2 *Sub Clock Input Characteristics*

(V_{CC} = 1.65V to 3.6V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input frequency	f_{CL}	X0A, X1A	-	-	32.768	-	kHz	When crystal oscillator is connected[1]
			-	32	-	100	kHz	When using external clock
Input clock cycle	t_{CYLL}		-	10	-	31.25	µs	When using external clock
Input clock pulse width	-		PWH/tCYLL, PWL/tCYLL	45	-	55	%	When using external clock

[1]. For more information about crystal oscillator, see Sub Crystal Oscillator in Handling Devices.



12.4.3 *Built-in CR Oscillation Characteristics*

12.4.3.1 Built-in High-speed CR

(V_{CC} = 1.65V to 3.6V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	f_{CRH}	T_A = + 25°C, V_{CC} ≥ 2.7V	3.94	4	4.06	MHz	When trimming[1]
		T_A = - 20°C to + 85°C, V_{CC} ≥ 2.7V	3.92	4	4.08		
		T_A = - 40°C to + 85°C, V_{CC} ≥ 2.7V	3.88	4	4.12		
		T_A = + 25°C, V_{CC} < 2.7V	3.9	4	4.1		
		T_A = - 40°C to + 85°C V_{CC} < 2.7V	3.66	4	4.20		
		T_A = - 40°C to + 85°C	2.8	4	5.2		When not trimming
Frequency stabilization time	t_{CRWT}	-	-	-	30	µs	[2]

[1]. In the case of using the values in CR trimming area of Flash memory at shipment for frequency/temperature trimming.

[2]. This is the time to stabilize the frequency of High-speed CR clock after setting trimming value. This period is able to use High-speed CR clock as source clock.

12.4.3.2 Built-in Low-speed CR

(V_{CC} = 1.65V to 3.6V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	f_{CRL}	-	50	100	150	kHz	

12.4.4 *Operating Conditions of Main PLL*

12.4.4.1 Operating Conditions of Main PLL (In the case of using main clock for input of Main PLL)

(V_{CC} = 1.65V to 3.6V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time[1] (LOCK UP time)	t_{LOCK}	100	-	-	µs	
PLL input clock frequency	f_{PLLI}	4	-	16	MHz	
PLL multiplication rate	-	5	-	37	multiplier	
PLL macro oscillation clock frequency	f_{PLLO}	75	-	150	MHz	
Main PLL clock frequency[2]	f_{CLKPLL}	-	-	40	MHz	

[1]. Time from when the PLL starts operating until the oscillation stabilizes.

[2]. For more information about Main PLL clock (CLKPLL), see Chapter 2-1: Clock in FM3 Family Peripheral Manual.

12.4.4.2 Operating Conditions of Main PLL (In the case of using the built-in High-speed CR for input clock of Main PLL)

(V_{CC} = 1.65V to 3.6V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time[1] (LOCK UP time)	t_{LOCK}	100	-	-	µs	
PLL input clock frequency	f_{PLLI}	3.8	4	4.2	MHz	
PLL multiplication rate	-	19	-	35	multiplier	
PLL macro oscillation clock frequency	f_{PLLO}	72	-	150	MHz	
Main PLL clock frequency[2]	f_{CLKPLL}	-	-	40	MHz	

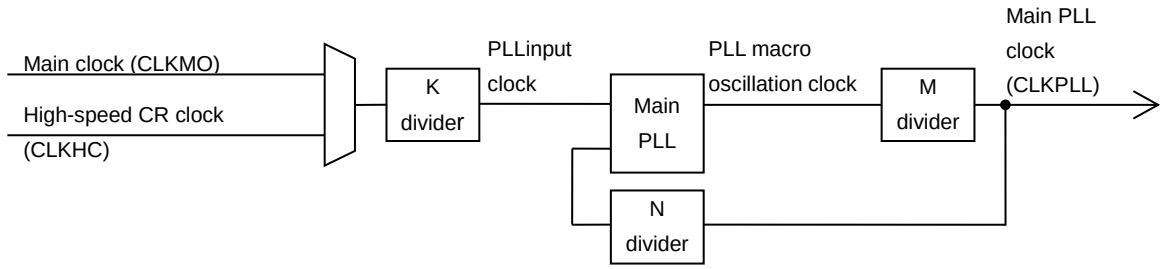
[1]. Time from when the PLL starts operating until the oscillation stabilizes.

[2]. For more information about Main PLL clock (CLKPLL), see Chapter 2-1: Clock in FM3 Family Peripheral Manual.

Note:

- Make sure to input to the Main PLL source clock, the High-speed CR clock (CLKHC) that the frequency has been trimmed.
- When setting PLL multiple rate, please take the accuracy of the built-in High-speed CR clock into account and prevent the master clock from exceeding the maximum frequency.

Main PLL connection



12.4.5 *Reset Input Characteristics*

(V_{CC} = 1.65V to 3.6V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Reset input time	t_{INITX}	INITX	-	500	-	ns	

12.4.6 *Power-on Reset Timing*

(Vss = 0V, T_A = - 40°C to + 85°C)

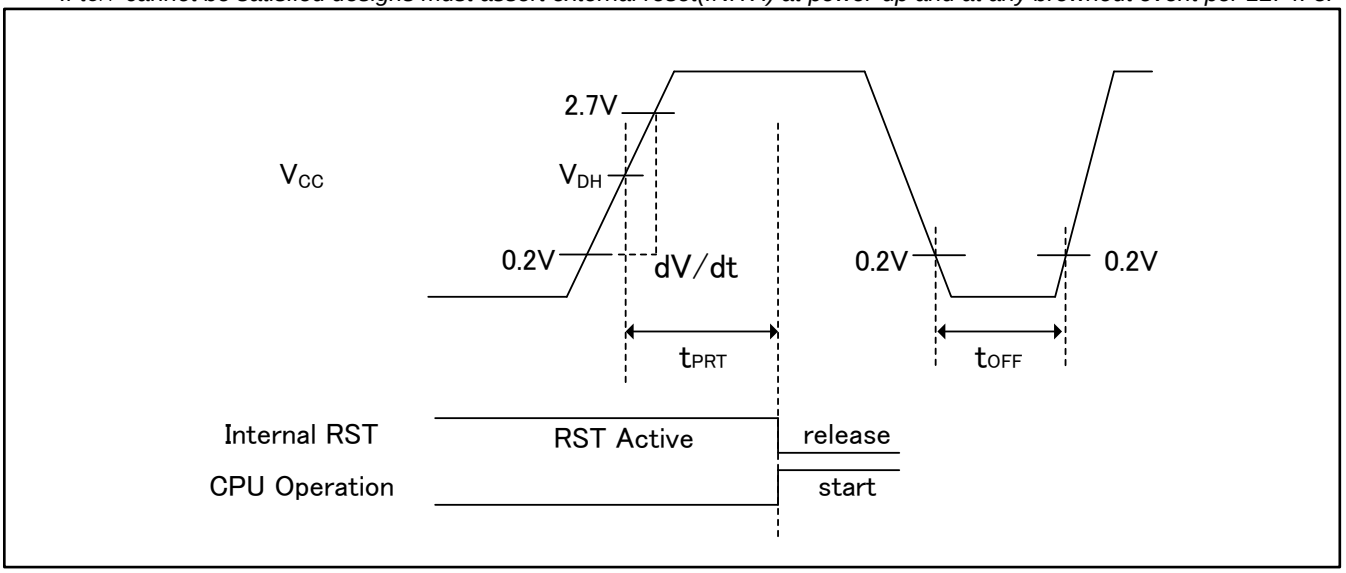
Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply shut down time	t_{OFF}	VCC	-	1	-	-	ms	*1
Power ramp rate	dV/dt		Vcc:0.2V to 2.70V	0.9	-	1000	mV/us	*2
Time until releasing Power-on reset	t_{PRT}		-	0.446	-	0.744	ms	

*1: V_{CC} must be held below 0.2V for minimum period of t_{OFF}. Improper initialization may occur if this condition is not met.

*2: This dV/dt characteristic is applied at the power-on of cold start (t_{OFF}>1ms).

Note:

- *If t_{OFF} cannot be satisfied designs must assert external reset(INITX) at power-up and at any brownout event per 12. 4. 5.*



Glossary

VDH: detection voltage of Low Voltage detection reset. See “12.6 Low-Voltage Detection Characteristics”

12.4.7 *External Bus Timing*

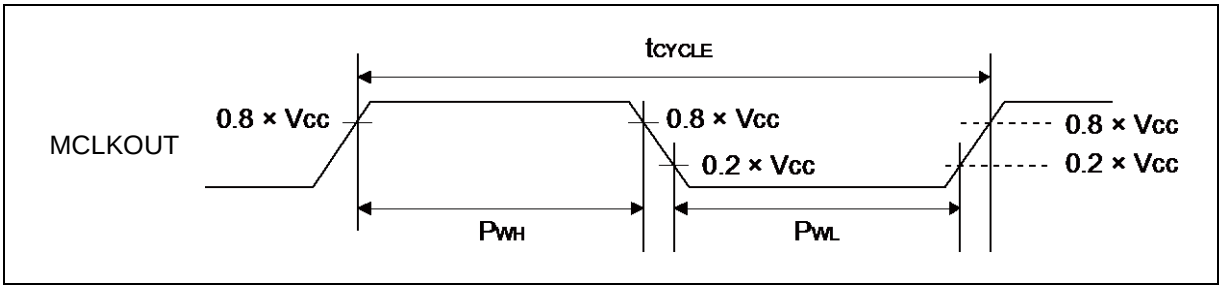
12.4.7.1 External bus clock output characteristics

(V_{CC} = 1.65V to 3.6V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Output frequency	t_{CYCLE}	MCLKOUT[1]	$V_{CC} \geq 2.7$ V	-	40	MHz
			$V_{CC} < 2.7$ V	-	20	MHz

The external bus clock (MCLKOUT) is a divided clock of HCLK. For more information about setting of clock divider, see Chapter 12: External Bus Interface in FM3 Family Peripheral Manual..

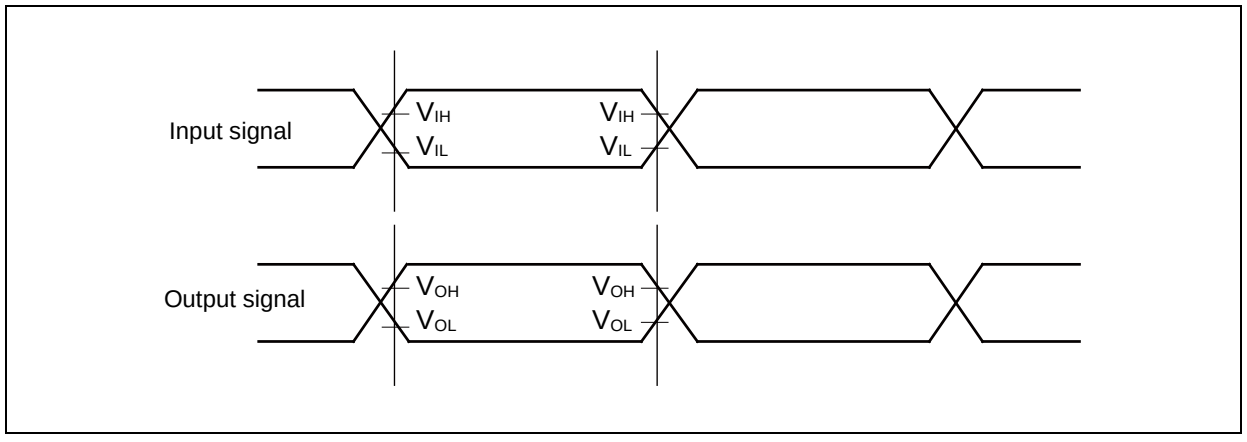
When external bus clock is not output, this characteristic does not give any effect on external bus operation.



12.4.7.2 External bus signal input/output characteristics

(V_{CC} = 1.65V to 3.6V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Conditions	Value	Unit	Remarks
Signal input characteristics	V_{IH}	-	0.8 × V_{CC}	V	
	V_{IL}		0.2 × V_{CC}	V	
Signal output characteristics	V_{OH}		0.8 × V_{CC}	V	
	V_{OL}		0.2 × V_{CC}	V	



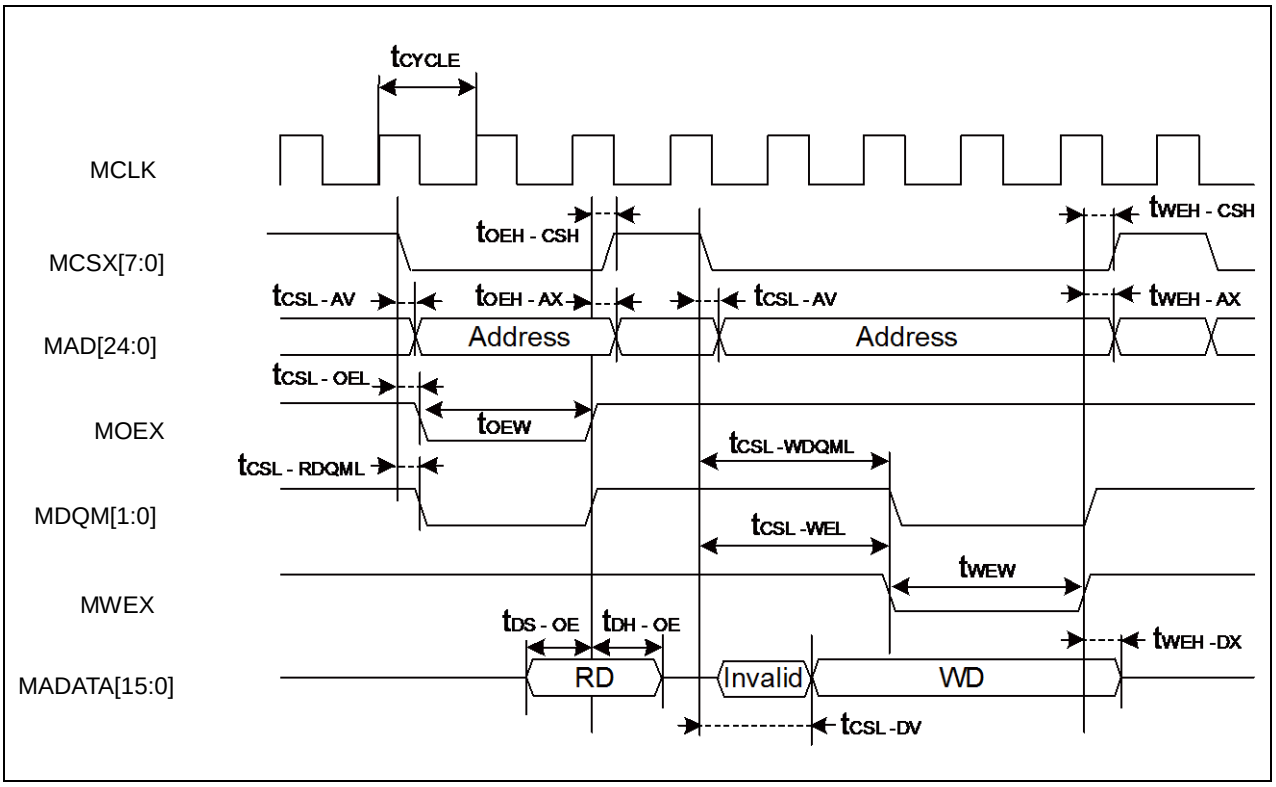
12.4.7.3 Separate Bus Access Asynchronous SRAM Mode

(V_{CC} = 1.65V to 3.6V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
MOEX Min pulse width	t_{OEW}	MOEX	$V_{CC} \geq 2.7$ V	MCLK×n-3	-	ns
			$V_{CC} < 2.7$ V			
MCSX ↓ → Address output delay time	$t_{CSL - AV}$	MCSX[7:0], MAD[24:0]	$V_{CC} \geq 2.7$ V	-9	+9	ns
			$V_{CC} < 2.7$ V	-12	+12	
MOEX ↑ → Address hold time	$t_{OEH - AX}$	MOEX, MAD[24:0]	$V_{CC} \geq 2.7$ V	0	MCLK×m+9	ns
			$V_{CC} < 2.7$ V		MCLK×m+12	
MCSX ↓ →MOEX ↓ delay time	$t_{CSL - OEL}$	MOEX, MCSX[7:0]	$V_{CC} \geq 2.7$ V	MCLK×m-9	MCLK×m+9	ns
			$V_{CC} < 2.7$ V	MCLK×m-12	MCLK×m+12	
MOEX ↑ → MCSX ↑ time	$t_{OEH - CSH}$		$V_{CC} \geq 2.7$ V	0	MCLK×m+9	ns
			$V_{CC} < 2.7$ V		MCLK×m+12	
MCSX ↓ → MDQM ↓ delay time	$t_{CSL - RDQML}$	MCSX, MDQM[1:0]	$V_{CC} \geq 2.7$ V	MCLK×m-9	MCLK×m+9	ns
			$V_{CC} < 2.7$ V	MCLK×m-12	MCLK×m+12	
Data set up → MOEX ↑ time	$t_{DS - OE}$	MOEX, MADATA[15:0]	$V_{CC} \geq 2.7$ V	20	-	ns
			$V_{CC} < 2.7$ V	38	-	
MOEX ↑ →Data hold time	$t_{DH - OE}$	MOEX, MADATA[15:0]	$V_{CC} \geq 2.7$ V	0	-	ns
			$V_{CC} < 2.7$ V			
MWEX Min pulse width	t_{WEW}	MWEX	$V_{CC} \geq 2.7$ V	MCLK×n-3	-	ns
			$V_{CC} < 2.7$ V			
MWEX ↑ → Address output delay time	$t_{WEH - AX}$	MWEX, MAD[24:0]	$V_{CC} \geq 2.7$ V	0	MCLK×m+9	ns
			$V_{CC} < 2.7$ V		MCLK×m+12	
MCSX ↓ → MWEX ↓ delay time	$t_{CSL - WEL}$	MWEX, MCSX[7:0]	$V_{CC} \geq 2.7$ V	MCLK×n-9	MCLK×n+9	ns
			$V_{CC} < 2.7$ V	MCLK×n-12	MCLK×n+12	
MWEX ↑ → MCSX ↑ delay time	$t_{WEH - CSH}$		$V_{CC} \geq 2.7$ V	0	MCLK×m+9	ns
			$V_{CC} < 2.7$ V		MCLK×m+12	
MCSX ↓→ MDQM ↓ delay time	$t_{CSL-WDQML}$	MCSX, MDQM[1:0]	$V_{CC} \geq 2.7$ V	MCLK×n-9	MCLK×n+9	ns
			$V_{CC} < 2.7$ V	MCLK×n-12	MCLK×n+12	
MCSX ↓→ Data output time	t_{CSL-DV}	MCSX, MADATA[15:0]	$V_{CC} \geq 2.7$ V	MCLK-9	MCLK+9	ns
			$V_{CC} < 2.7$ V	MCLK-12	MCLK+12	
MWEX ↑ → Data hold time	$t_{WEH - DX}$	MWEX, MADATA[15:0]	$V_{CC} \geq 2.7$ V	0	MCLK×m+9	ns
			$V_{CC} < 2.7$ V		MCLK×m+12	

Note:

When the external load capacitance C_L = 30 pF (m = 0 to 15, n = 1 to 16).


tCYCLE
MCLK
MCSX[7:0]
MAD[24:0]
MOEX
MDQM[1:0]
MWEX
MADATA[15:0]
tOEH - CSH
tWEH - CSH
tCSL - AV
tOEH - AX
tCSL - AV
tWEH - AX
Address
Address
tCSL - OEL
tOEW
tCSL - RDQML
tCSL -WDQML
tCSL -WEL
tWEW
tDS - OE
tDH - OE
tWEH -DX
RD
Invalid
WD
tCSL -DV

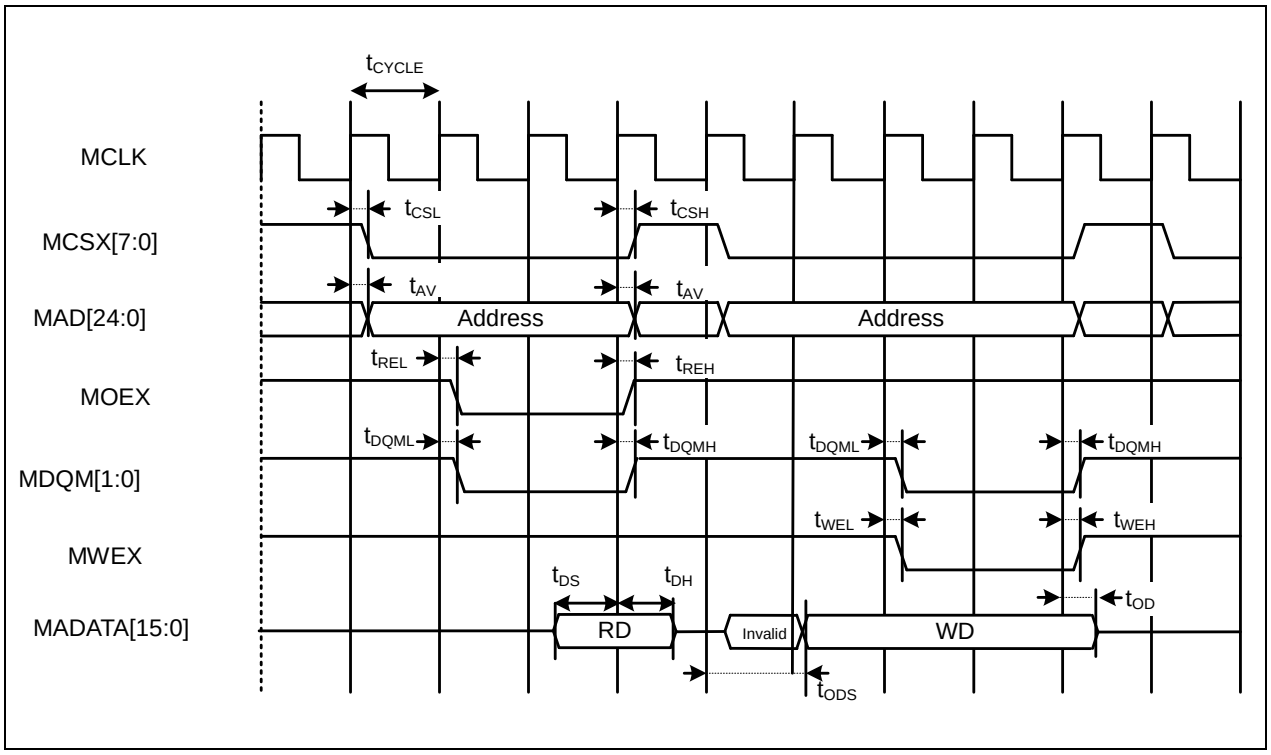
12.4.7.4 Separate Bus Access Synchronous SRAM Mode

(V_{CC} = 1.65V to 3.6V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Address delay time	t_{AV}	MCLK, MAD[24:0]	$V_{CC} \geq 2.7$ V	1	9	ns
			$V_{CC} < 2.7$ V		12	
MCSX delay time	t_{CSL}	MCLK, MCSX[7:0]	$V_{CC} \geq 2.7$ V	1	9	ns
			$V_{CC} < 2.7$ V		12	
	t_{CSH}		$V_{CC} \geq 2.7$ V	1	9	ns
			$V_{CC} < 2.7$ V		12	
MOEX delay time	t_{REL}	MCLK, MOEX	$V_{CC} \geq 2.7$ V	1	9	ns
			$V_{CC} < 2.7$ V		12	
	t_{REH}		$V_{CC} \geq 2.7$ V	1	9	ns
			$V_{CC} < 2.7$ V		12	
Data set up →MCLK ↑ time	t_{DS}	MCLK, MADATA[15:0]	$V_{CC} \geq 2.7$ V	19	-	ns
			$V_{CC} < 2.7$ V	37		
MCLK ↑ → Data hold time	t_{DH}	MCLK, MADATA[15:0]	$V_{CC} \geq 2.7$ V	0	-	ns
			$V_{CC} < 2.7$ V			
MWEX delay time	t_{WEL}	MCLK, MWEX	$V_{CC} \geq 2.7$ V	1	9	ns
			$V_{CC} < 2.7$ V		12	
	t_{WEH}		$V_{CC} \geq 2.7$ V	1	9	ns
			$V_{CC} < 2.7$ V		12	
MDQM[1:0] delay time	t_{DQML}	MCLK, MDQM[1:0]	$V_{CC} \geq 2.7$ V	1	9	ns
			$V_{CC} < 2.7$ V		12	
	t_{DQMH}		$V_{CC} \geq 2.7$ V	1	9	ns
			$V_{CC} < 2.7$ V		12	
MCLK ↑ → Data output time	t_{ODS}	MCLK, MADATA[15:0]	$V_{CC} \geq 2.7$ V	MCLK+1	MCLK+18	ns
			$V_{CC} < 2.7$ V		MCLK+24	
MCLK ↑ → Data hold time	t_{OD}	MCLK, MADATA[15:0]	$V_{CC} \geq 2.7$ V	1	18	ns
			$V_{CC} < 2.7$ V		24	

Note:

- *When the external load capacitance C_L = 30 pF.*


tCYCLE
MCLK
MCSX[7:0]
MAD[24:0]
MOEX
MDQM[1:0]
MWEX
MADATA[15:0]
tCSL
tCSH
tAV
tAV
Address
Address
tREL
tREH
tDQML
tDQMH
tDQML
tDQMH
tWEL
tWEH
tDS
tDH
tOD
RD
Invalid
WD
tODS

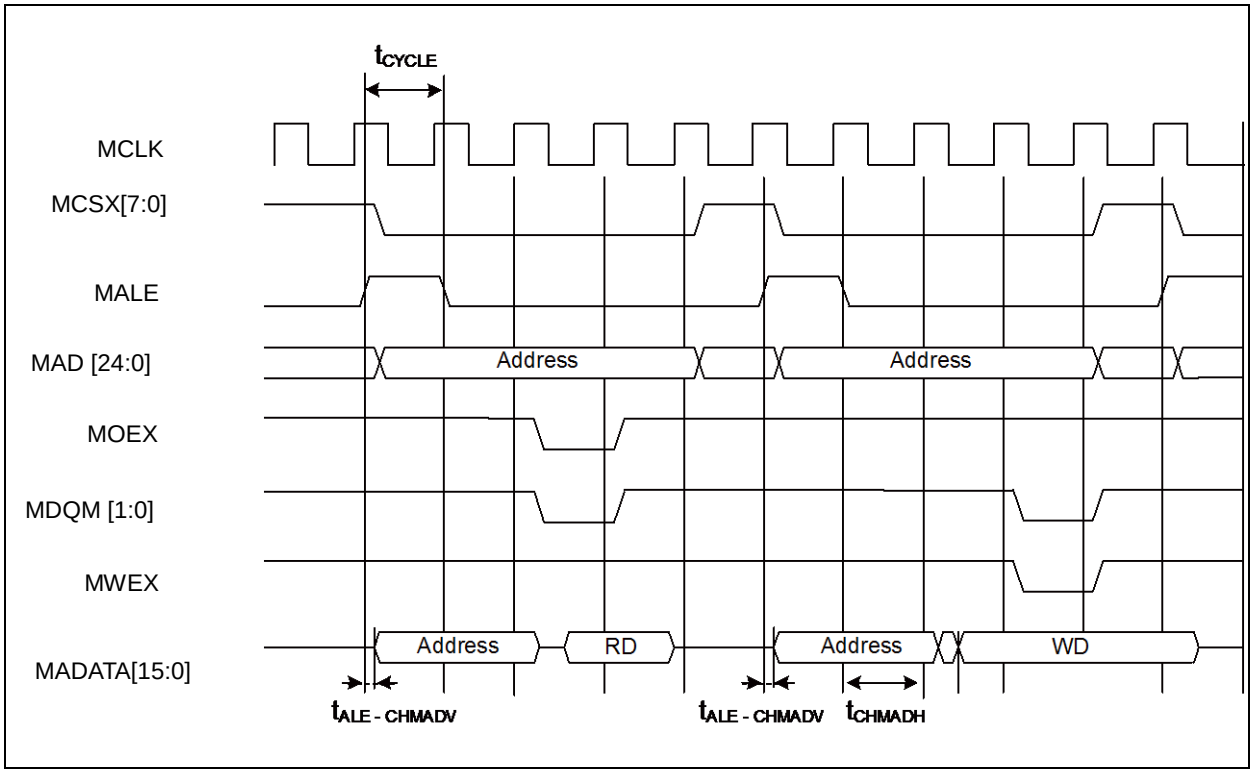
12.4.7.5 Multiplexed Bus Access Asynchronous SRAM Mode

(V_{CC} = 1.65V to 3.6V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Multiplexed address delay time	$t_{ALE-CHMADV}$	MALE, MADATA[15:0]	$V_{CC} \geq 2.7$ V	0	+10	ns
			$V_{CC} < 2.7$ V		+20	
Multiplexed address hold time	t_{CHMADH}		$V_{CC} \geq 2.7$ V	MCLK×n+0	MCLK×n+10	ns
			$V_{CC} < 2.7$ V	MCLK×n+0	MCLK×n+20	

Note:

- *When the external load capacitance C_L = 30 pF (m = 0 to 15, n = 1 to 16).*



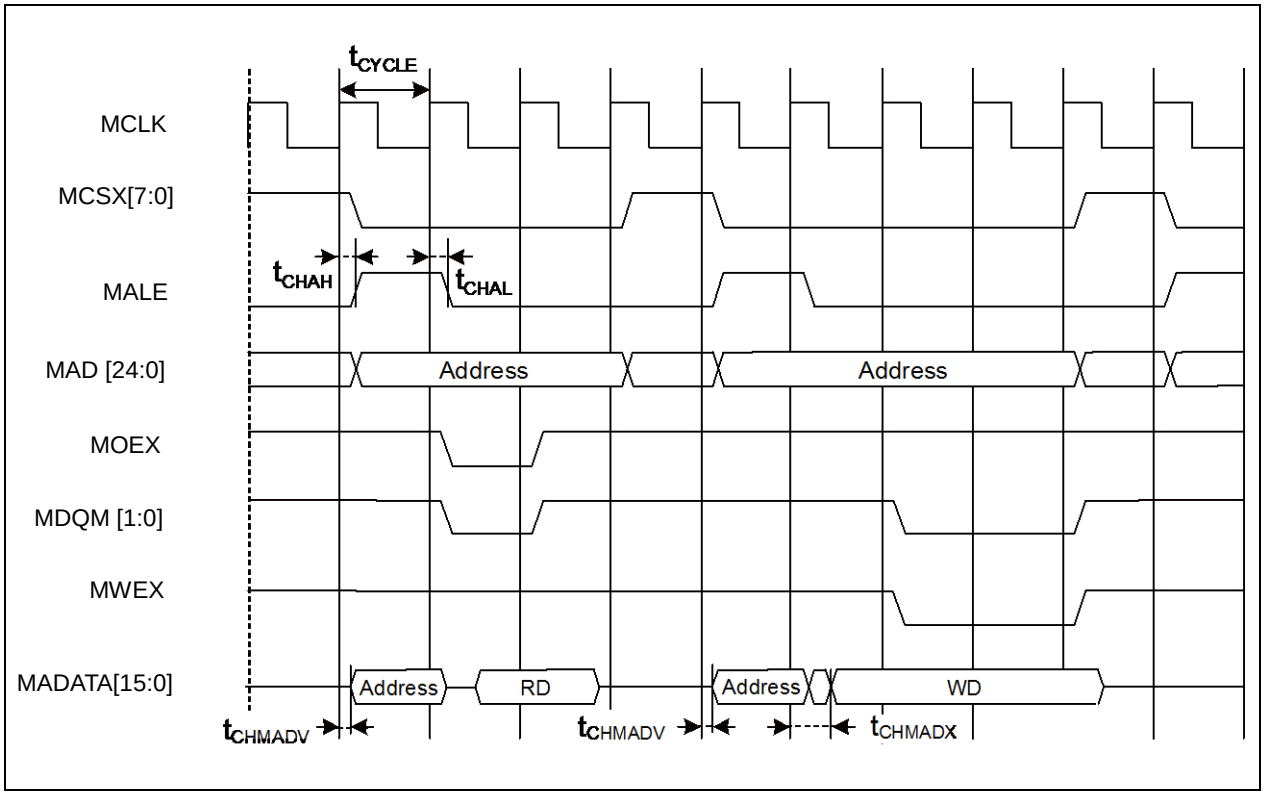
12.4.7.6 Multiplexed Bus Access Synchronous SRAM Mode

(V_{CC} = 1.65V to 3.6V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
MALE delay time	t_{CHAL}	MCLK, ALE	$V_{CC} \geq 2.7$ V	1	9	ns	
			$V_{CC} < 2.7$ V		12	ns	
	t_{CHAH}		$V_{CC} \geq 2.7$ V	1	9	ns	
			$V_{CC} < 2.7$ V		12	ns	
MCLK ↑ → Multiplexed Address delay time	t_{CHMADV}	MCLK, MADATA[15:0]	$V_{CC} \geq 2.7$ V	1	t_{OD}	ns	
			$V_{CC} < 2.7$ V				
MCLK ↑ → Multiplexed Data output time	t_{CHMADX}		$V_{CC} \geq 2.7$ V	1	t_{OD}	ns	
			$V_{CC} < 2.7$ V				

Note:

- *When the external load capacitance C_L = 30 pF.*



12.4.7.7 NAND Flash Memory Mode

(V_{CC} = 1.65V to 3.6V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
MNREX Min pulse width	t_{NREW}	MNREX	$V_{CC} \geq 2.7$ V	MCLK×n-3	-	ns
			$V_{CC} < 2.7$ V			
Data setup → MNREX↑time	t_{DS-NRE}	MNREX, MADATA[15:0]	$V_{CC} \geq 2.7$ V	20	-	ns
			$V_{CC} < 2.7$ V	38	-	
MNREX↑→ Data hold time	t_{DH-NRE}	MNREX, MADATA[15:0]	$V_{CC} \geq 2.7$ V	0	-	ns
			$V_{CC} < 2.7$ V			
MNALE↑→MNWEX delay time	$t_{ALEH-NWEL}$	MNALE, MNWEX	$V_{CC} \geq 2.7$ V	MCLK×m-9	MCLK×m+9	ns
			$V_{CC} < 2.7$ V	MCLK×m-12	MCLK×m+12	
MNALE↓→MNWEX delay time	$t_{ALEL-NWEL}$	MNALE, MNWEX	$V_{CC} \geq 2.7$ V	MCLK×m-9	MCLK×m+9	ns
			$V_{CC} < 2.7$ V	MCLK×m-12	MCLK×m+12	
MNCLE↑→MNWEX delay time	$t_{CLEH-NWEL}$	MNCLE, MNWEX	$V_{CC} \geq 2.7$ V	MCLK×m-9	MCLK×m+9	ns
			$V_{CC} < 2.7$ V	MCLK×m-12	MCLK×m+12	
MNWEX↑→MNCLE delay time	$t_{NWEH-CLEL}$	MNCLE, MNWEX	$V_{CC} \geq 2.7$ V	0	MCLK×m+9	ns
			$V_{CC} < 2.7$ V		MCLK×m+12	
MNWEX Min pulse width	t_{NWEW}	MNWEX	$V_{CC} \geq 2.7$ V	MCLK×n-3	-	ns
			$V_{CC} < 2.7$ V			
MNWEX↓→Data output time	$t_{NWEL-DV}$	MNWEX, MADATA[15:0]	$V_{CC} \geq 2.7$ V	- 9	+ 9	ns
			$V_{CC} < 2.7$ V	-12	+12	
MNWEX↑→Data hold time	$t_{NWEH-DX}$	MNWEX, MADATA[15:0]	$V_{CC} \geq 2.7$ V	0	MCLK×m+9	ns
			$V_{CC} < 2.7$ V		MCLK×m+12	

Note:

- *When the external load capacitance C_L = 30 pF (m=0 to 15, n=1 to 16).*

Figure 1. NAND Flash Memory Read

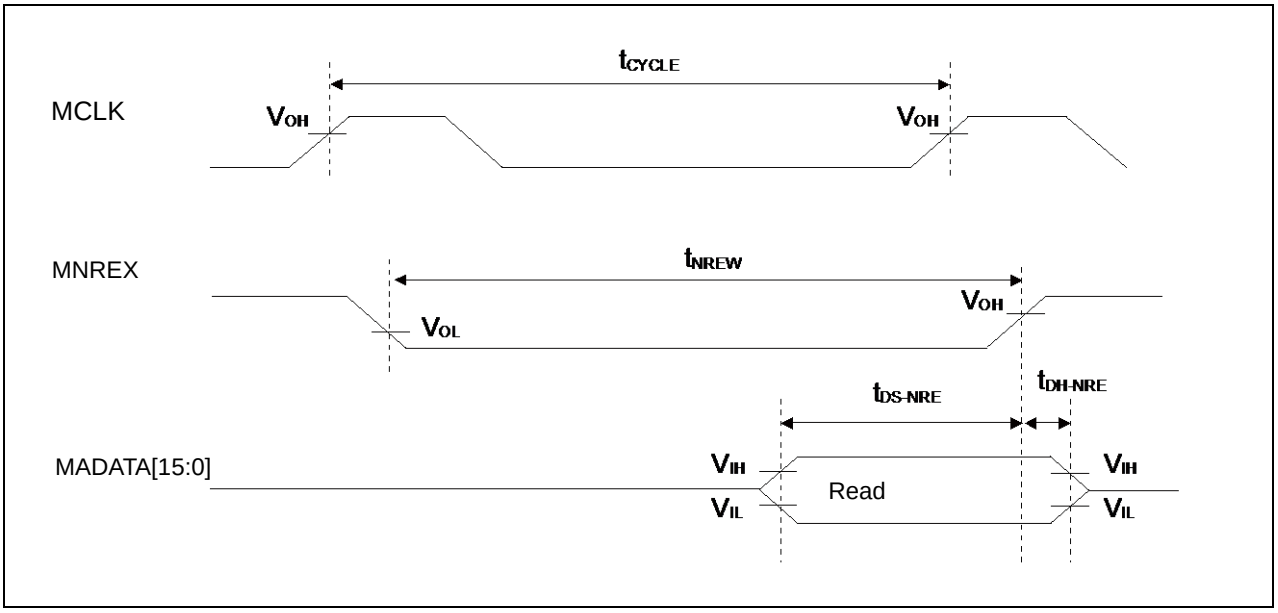


Figure 2. NAND Flash Memory Address Write

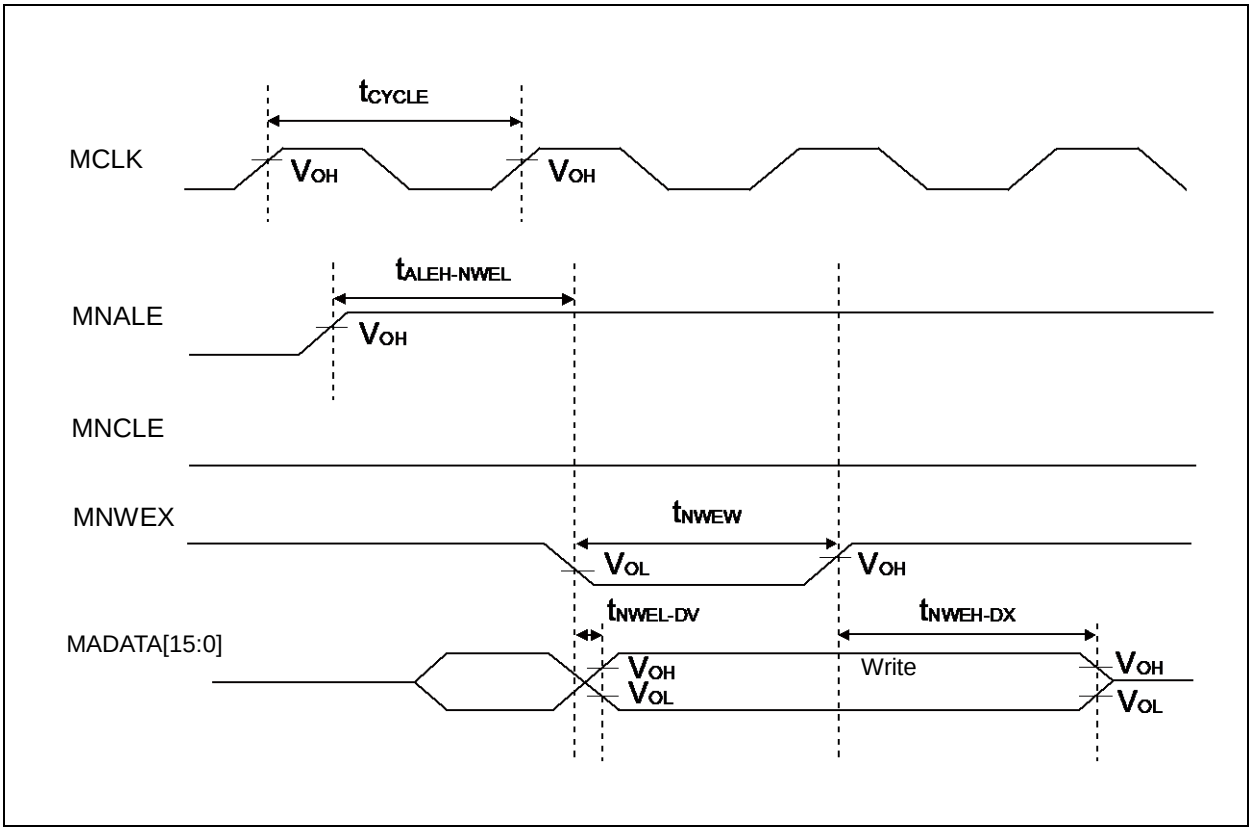
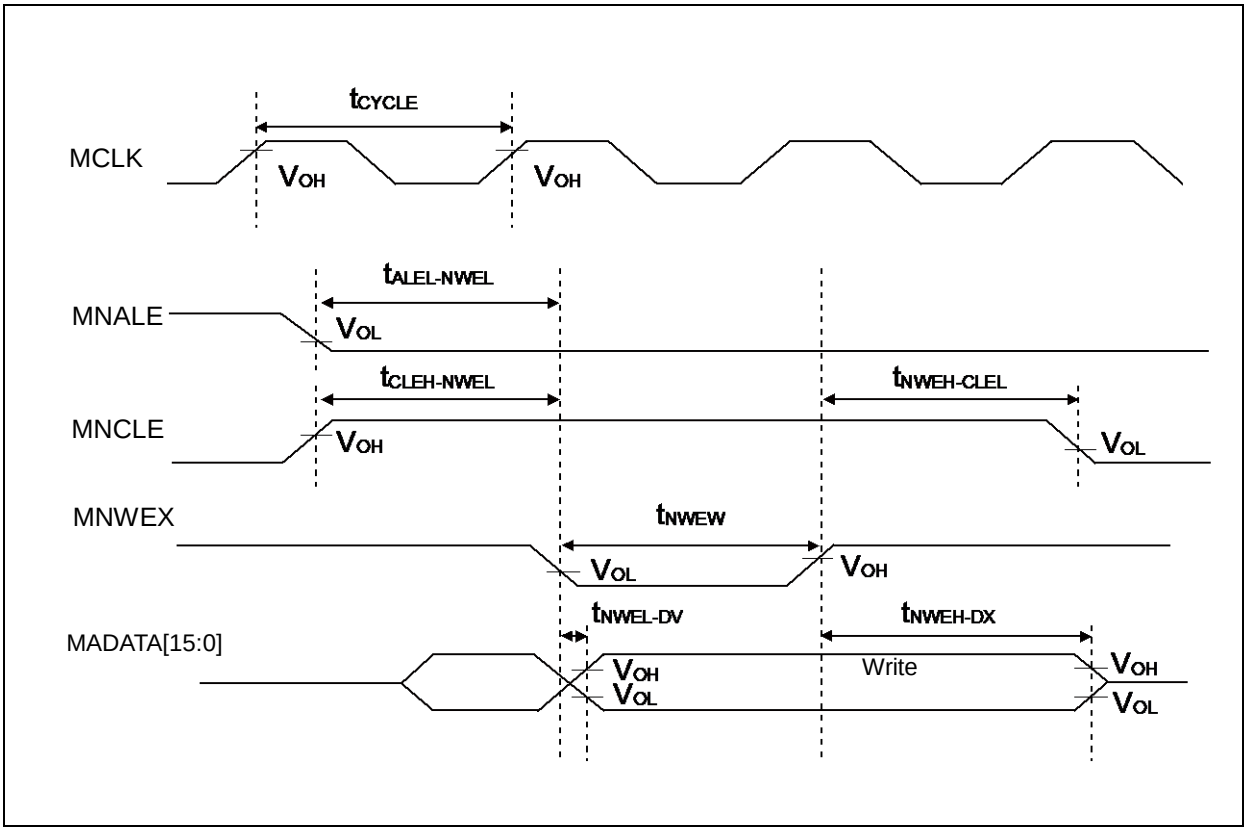


Figure 3. NAND Flash Memory Command Write

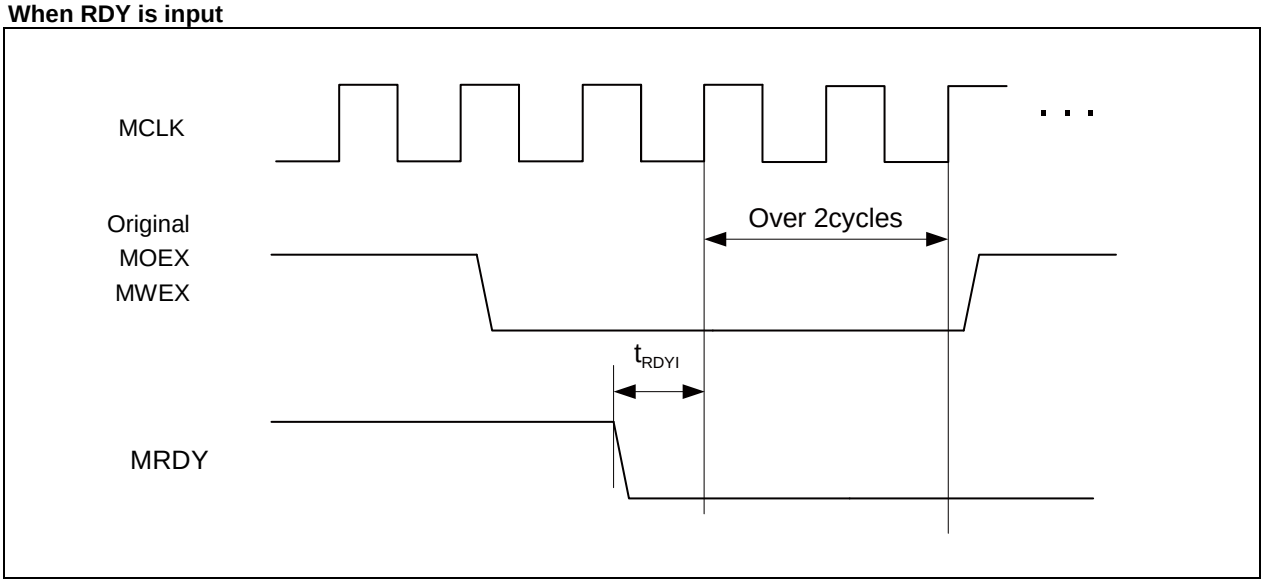


12.4.7.8 External Ready Input Timing

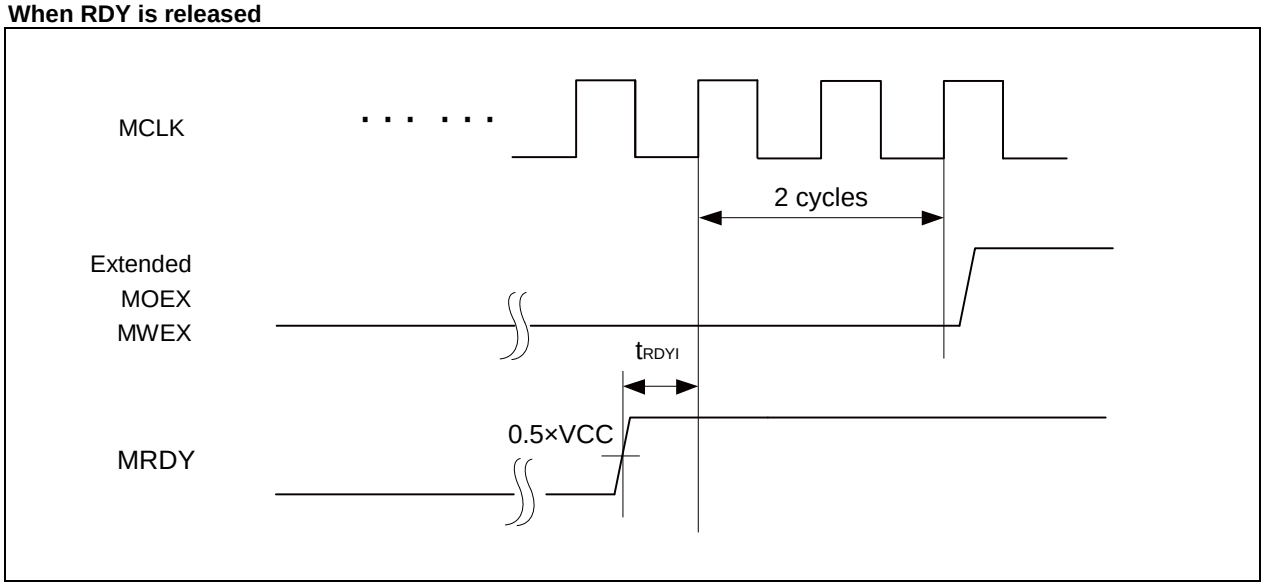
(V_{CC} = 1.65V to 3.6V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
MCLK ↑ MRDY input setup time	t_{RDYI}	MCLK, MRDY	$V_{CC} \geq 2.7$ V	19	-	ns	
			$V_{CC} < 2.7$ V	37			

When RDY is input



When RDY is released

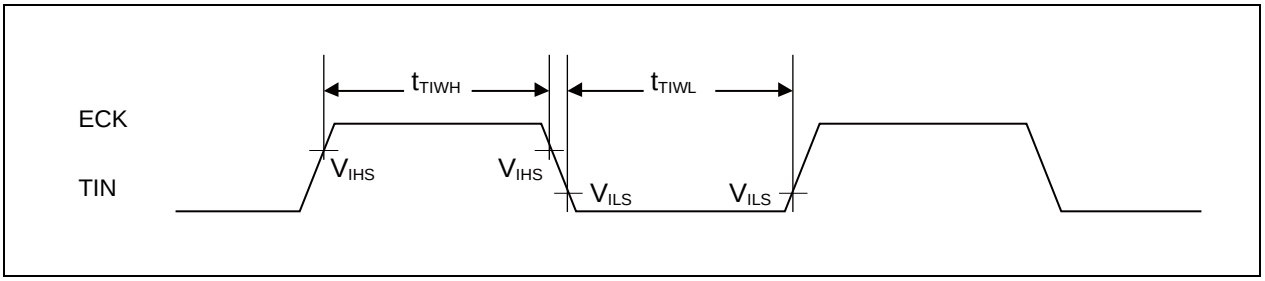


12.4.8 *Base Timer Input Timing*

12.4.8.1 Timer input timing

(V_{CC} = 1.65V to 3.6V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

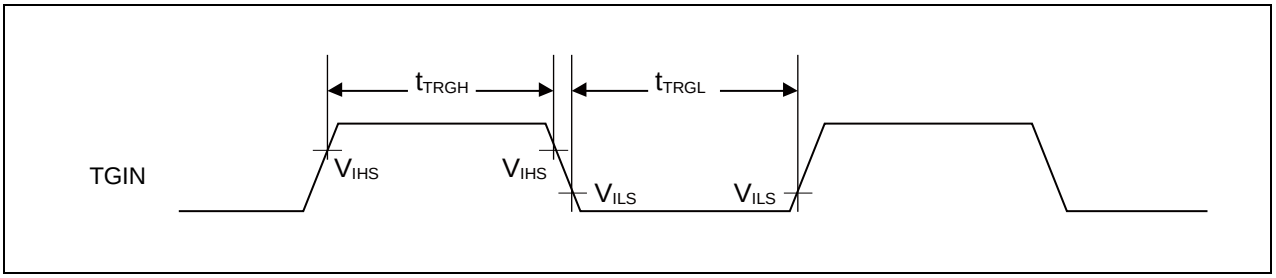
Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TIWH}, t_{TIWL}	TIOAn/TIOBn (when using as ECK, TIN)	-	$2t_{CYCP}$	-	ns	



12.4.8.2 Trigger input timing

(V_{CC} = 1.65V to 3.6V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TRGH}, t_{TRGL}	TIOAn/TIOBn (when using as TGIN)	-	$2t_{CYCP}$	-	ns	



Note:

- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which the Base Timer is connected to, see Block Diagram in this data sheet.

12.4.9 *CSIO/UART Timing*

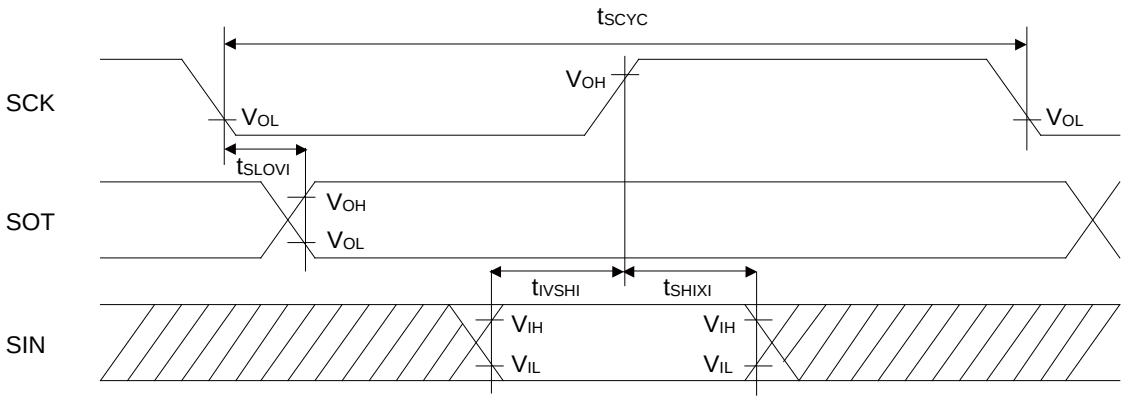
12.4.9.1 CSIO (SPI = 0, SCINV = 0)

(V_{CC} = 1.65V to 3.6V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

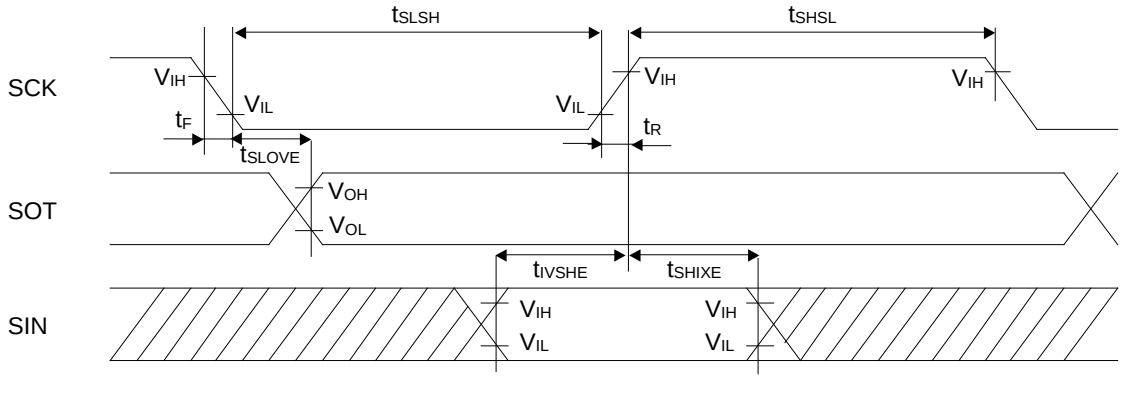
Parameter	Symbol	Pin name	Conditions	V_{CC} < 2.7 V		$V_{CC} \geq$ 2.7 V		Unit
				Min	Max	Min	Max	
Baud rate	-	-	-	-	8	-	8	Mbps
Serial clock cycle time	t_{SCYC}	SCKx	Master mode	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN → SCK ↑ setup time	t_{IVSHI}	SCKx, SINx		50	-	30	-	ns
SCK ↑ → SIN hold time	t_{SHIXI}	SCKx, SINx		0	-	0	-	ns
Serial clock L pulse width	t_{SLSH}	SCKx	Slave mode	$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	ns
Serial clock H pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK ↓ → SOT delay time	t_{SLOVE}	SCKx, SOTx		-	50	-	30	ns
SIN → SCK ↑ setup time	t_{IVSHE}	SCKx, SINx		10	-	10	-	ns
SCK ↑ → SIN hold time	t_{SHIXE}	SCKx, SINx		20	-	20	-	ns
SCK falling time	t_F	SCKx		-	5	-	5	ns
SCK rising time	t_R	SCKx		-	5	-	5	ns

Notes:

- *The above characteristics apply to clock synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time. About the APB bus number which Multi-function Serial is connected to, see Block Diagram in this data sheet.*
- *These characteristics only guarantee the same relocate port number.*
  For example, the combination of SCKx_0 and SOTx_1 is not guaranteed.
- *When the external load capacitance C_L = 30 pF.*



Master mode



Slave mode

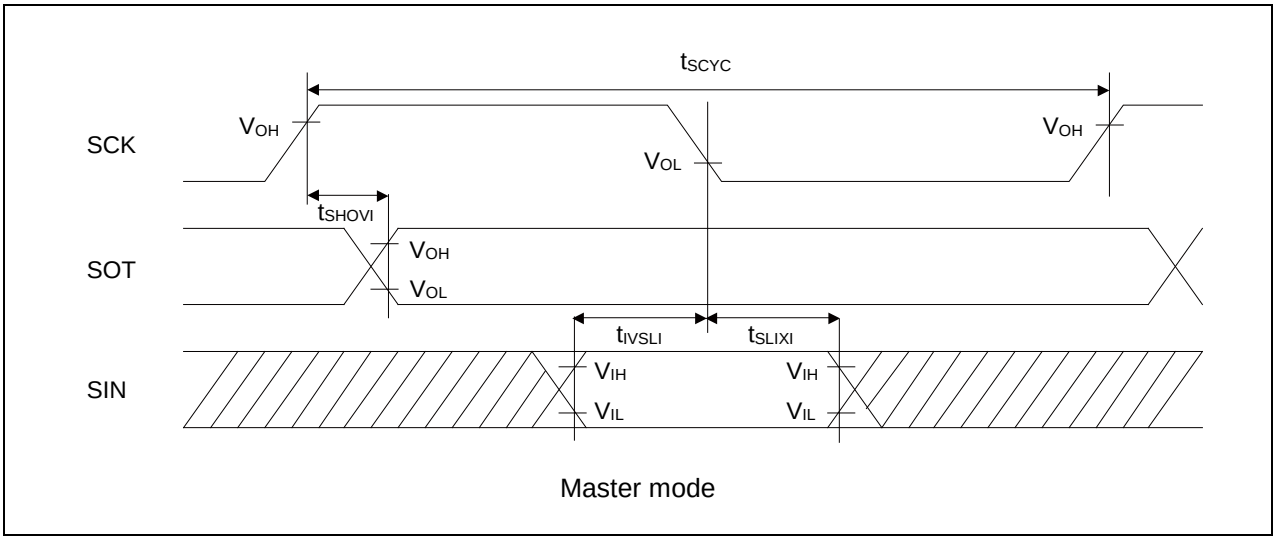
12.4.9.2 CSIO (SPI = 0, SCINV = 1)

(V_{CC} = 1.65V to 3.6V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

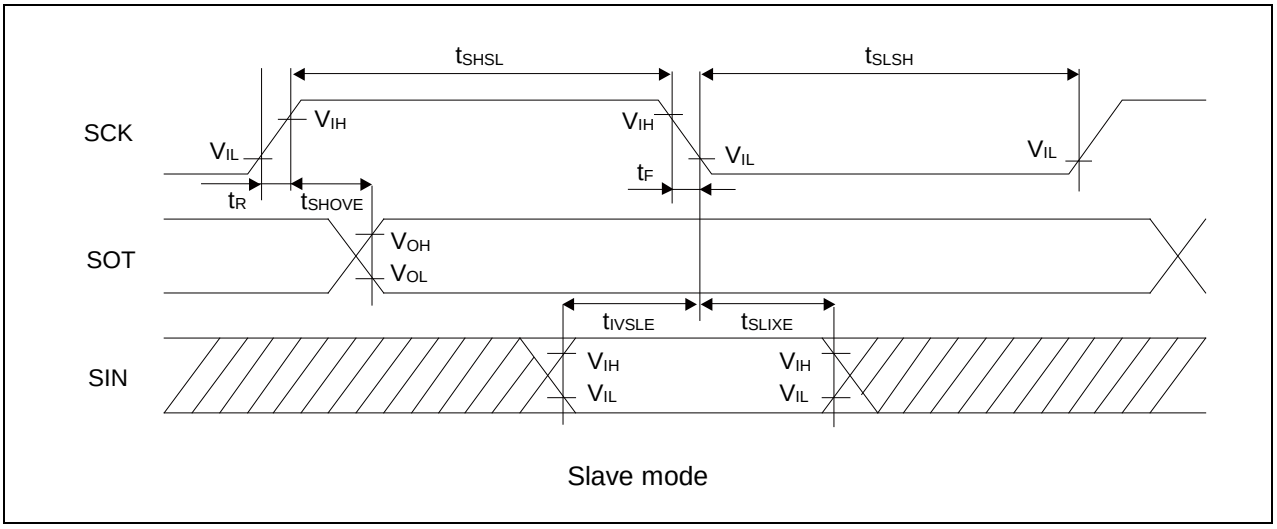
Parameter	Symbol	Pin name	Conditions	V_{CC} < 2.7 V		V_{CC} ≧ 2.7 V		Unit
				Min	Max	Min	Max	
Baud rate	-	-	-	-	8	-	8	Mbps
Serial clock cycle time	t_{SCYC}	SCKx	Master mode	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK ↑ → SOT delay time	t_{SHOVI}	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN → SCK ↓ setup time	t_{IVSLI}	SCKx, SINx		50	-	30	-	ns
SCK ↓ → SIN hold time	t_{SLIXI}	SCKx, SINx		0	-	0	-	ns
Serial clock L pulse width	t_{SLSH}	SCKx	Slave mode	$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	ns
Serial clock H pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK ↑ → SOT delay time	t_{SHOVE}	SCKx, SOTx		-	50	-	30	ns
SIN → SCK ↓ setup time	t_{IVSLE}	SCKx, SINx		10	-	10	-	ns
SCK ↓ → SIN hold time	t_{SLIXE}	SCKx, SINx		20	-	20	-	ns
SCK falling time	t_F	SCKx		-	5	-	5	ns
SCK rising time	t_R	SCKx		-	5	-	5	ns

Notes:

- *The above characteristics apply to clock synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time. About the APB bus number which Multi-function Serial is connected to, see Block Diagram in this data sheet.*
- *These characteristics only guarantee the same relocate port number.*
  For example, the combination of SCKx_0 and SOTx_1 is not guaranteed.
- *When the external load capacitance C_L = 30 pF.*



Master mode



Slave mode

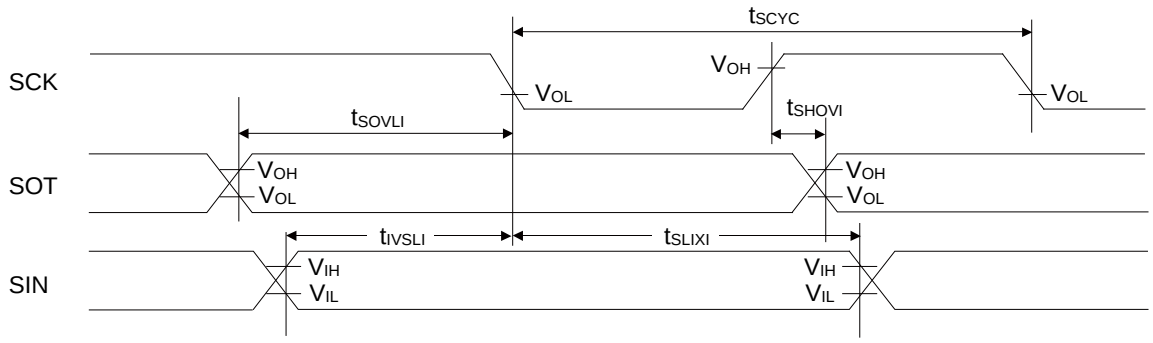
12.4.9.3 CSIO (SPI = 1, SCINV = 0)

(V_{CC} = 1.65V to 3.6V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

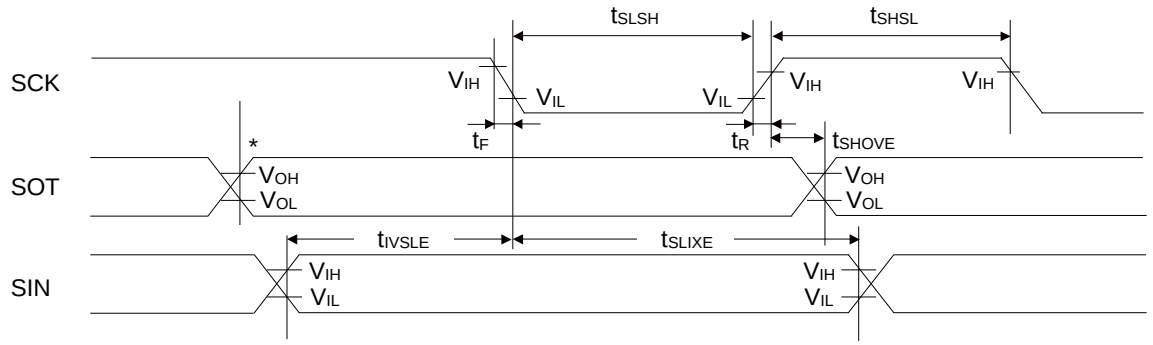
Parameter	Symbol	Pin name	Conditions	V_{CC} < 2.7 V		V_{CC} ≥ 2.7 V		Unit
				Min	Max	Min	Max	
Baud rate	-	-	-	-	8	-	8	Mbps
Serial clock cycle time	t_{SCYC}	SCKx	Master mode	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK ↑ → SOT delay time	t_{SHOVI}	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN → SCK ↓ setup time	t_{IVSLI}	SCKx, SINx		50	-	30	-	ns
SCK ↓→ SIN hold time	t_{SLIXI}	SCKx, SINx		0	-	0	-	ns
SOT → SCK ↓ delay time	t_{SOVLI}	SCKx, SOTx		$2t_{CYCP}$ - 30	-	$2t_{CYCP}$ - 30	-	ns
Serial clock L pulse width	t_{SLSH}	SCKx	Slave mode	$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	ns
Serial clock H pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK ↑ → SOT delay time	t_{SHOVE}	SCKx, SOTx		-	50	-	30	ns
SIN → SCK ↓ setup time	t_{IVSLE}	SCKx, SINx		10	-	10	-	ns
SCK ↓→ SIN hold time	t_{SLIXE}	SCKx, SINx		20	-	20	-	ns
SCK falling time	t_F	SCKx		-	5	-	5	ns
SCK rising time	t_R	SCKx		-	5	-	5	ns

Notes:

- *The above characteristics apply to clock synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time.About the APB bus number which Multi-function Serial is connected to, see Block Diagram in this data sheet.*
- *These characteristics only guarantee the same relocate port number.*
  For example, the combination of SCKx_0 and SOTx_1 is not guaranteed.
- *When the external load capacitance C_L = 30 pF.*



Master mode



Slave mode

*: Changes when writing to TDR register

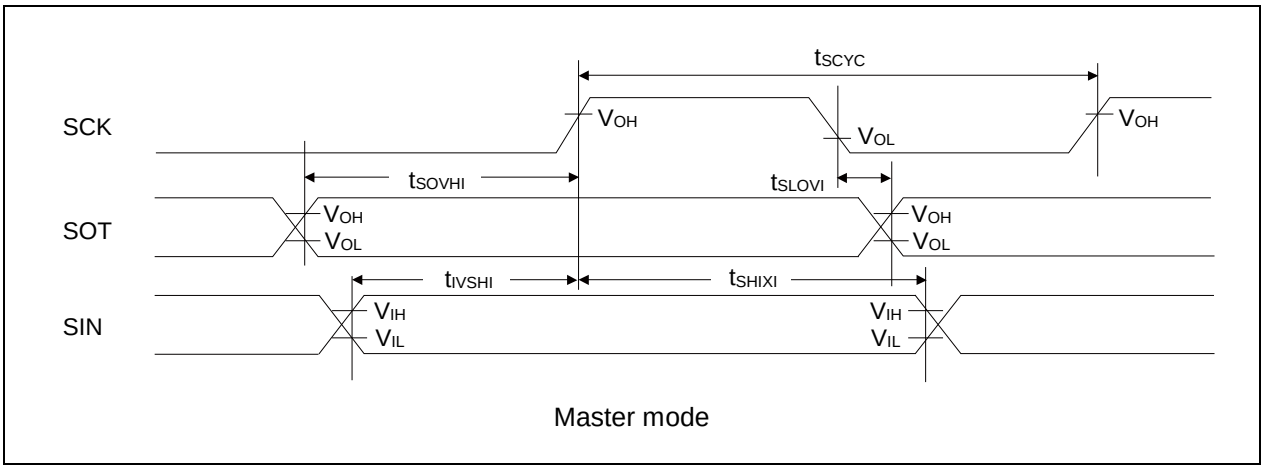
12.4.9.4 CSIO (SPI = 1, SCINV = 1)

(V_{CC} = 1.65V to 3.6V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

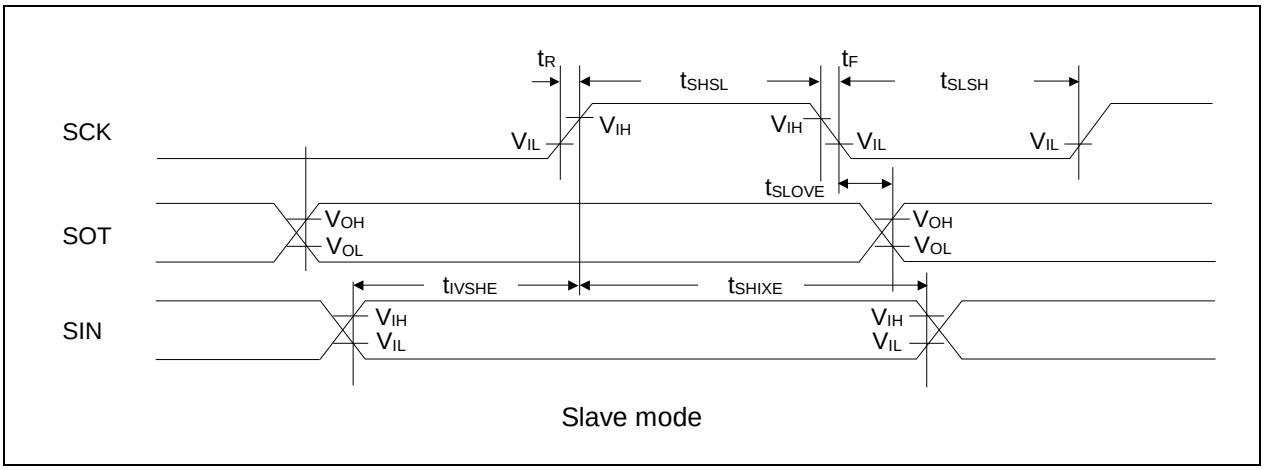
Parameter	Symbol	Pin name	Conditions	V_{CC} < 2.7 V		$V_{CC} \geq$ 2.7 V		Unit
				Min	Max	Min	Max	
Baud rate	-	-	-	-	8	-	8	Mbps
Serial clock cycle time	t_{SCYC}	SCKx	Master mode	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN → SCK ↑ setup time	t_{IVSHI}	SCKx, SINx		50	-	30	-	ns
SCK ↑ → SIN hold time	t_{SHIXI}	SCKx, SINx		0	-	0	-	ns
SOT → SCK ↑ delay time	t_{SOVHI}	SCKx, SOTx		$2t_{CYCP}$ - 30	-	$2t_{CYCP}$ - 30	-	ns
Serial clock L pulse width	t_{SLSH}	SCKx	Slave mode	$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	ns
Serial clock H pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK ↓ → SOT delay time	t_{SLOVE}	SCKx, SOTx		-	50	-	30	ns
SIN → SCK ↑ setup time	t_{IVSHE}	SCKx, SINx		10	-	10	-	ns
SCK ↑ → SIN hold time	t_{SHIXE}	SCKx, SINx		20	-	20	-	ns
SCK falling time	t_F	SCKx		-	5	-	5	ns
SCK rising time	t_R	SCKx		-	5	-	5	ns

Notes:

- *The above characteristics apply to clock synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time.About the APB bus number which Multi-function Serial is connected to, see Block Diagram in this data sheet.*
- *These characteristics only guarantee the same relocate port number.*
  For example, the combination of SCKx_0 and SOTx_1 is not guaranteed.
- *When the external load capacitance C_L = 30 pF.*



Master mode

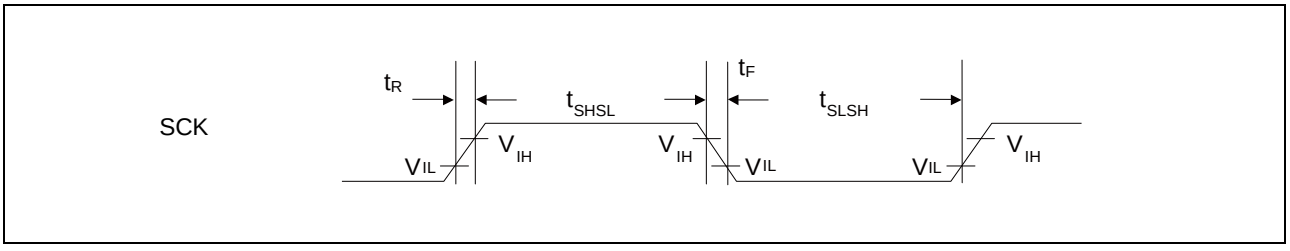


Slave mode

12.4.9.5 UART external clock input (EXT = 1)

(V_{CC} = 1.65V to 3.6V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Conditions	Value		Unit	Remarks
			Min	Max		
Serial clock L pulse width	t_{SLSH}	C_L = 30 pF	t_{CYCP} + 10	-	ns	
Serial clock H pulse width	t_{SHSL}		t_{CYCP} + 10	-	ns	
SCK falling time	t_F		-	5	ns	
SCK rising time	t_R		-	5	ns	

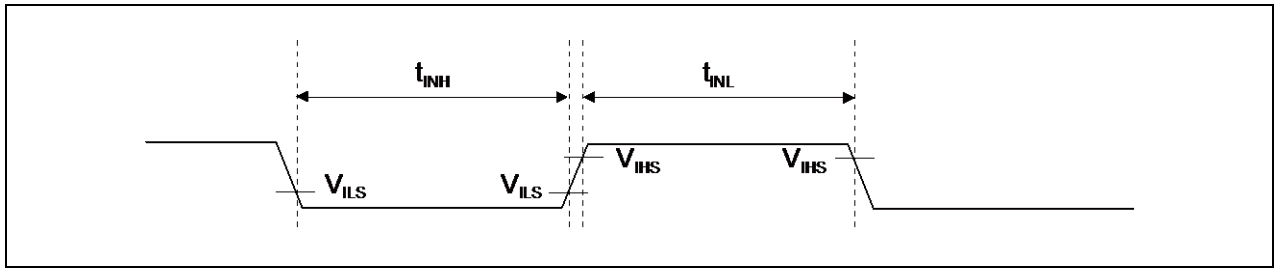


12.4.10 *External Input Timing*

(V_{CC} = 1.65V to 3.6V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{INH}, t_{INL}	ADTG	-	$2t_{CYCP}$[1]	-	ns	A/D converter trigger input
		FRCKx					Free-run timer input clock
		ICxx					Input capture
		DTIxX					Waveform generator
		INTxx, NMIX	[2]	$2t_{CYCP}$ + 100[1]	-	ns	External interrupt, NMI
			[3]	500	-	ns	
		WKUPx	[4]	600	-	ns	Deep Standby wake up

[1]. t_{CYCP} indicates the APB bus clock cycle time.
About the APB bus number which the Multi-function Timer is connected to, see Block Diagram in this data sheet.
[2]. When in Run mode, in Sleep mode.
[3]. When in Stop mode, in Timer mode.
[4]. When in Deep Standby RTC mode, in Deep Standby Stop mode.

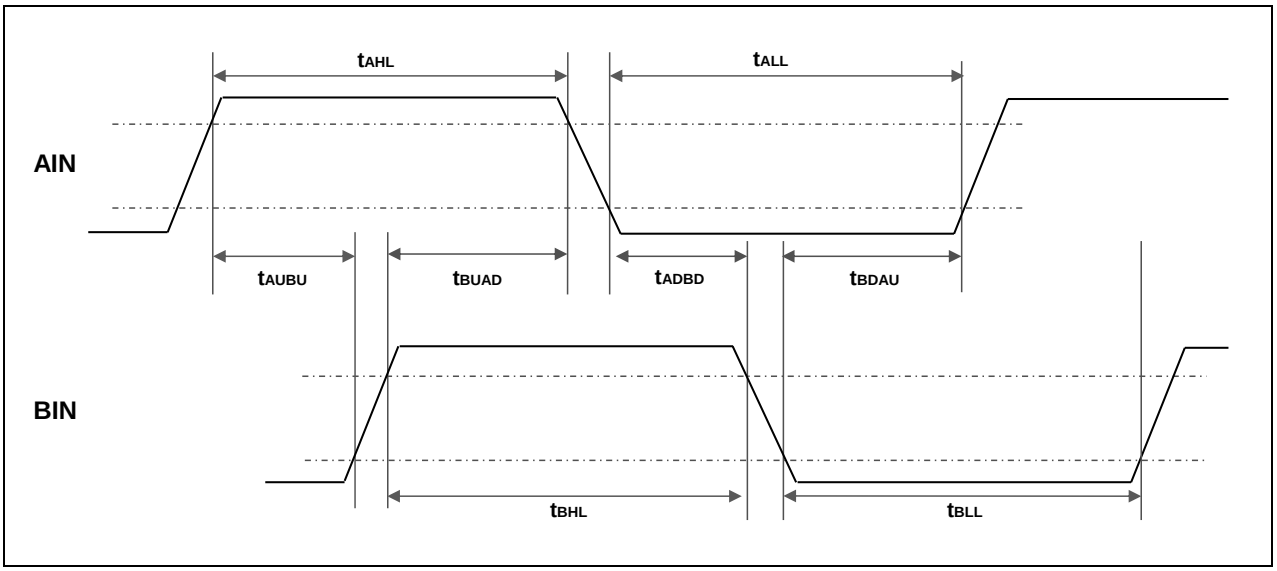


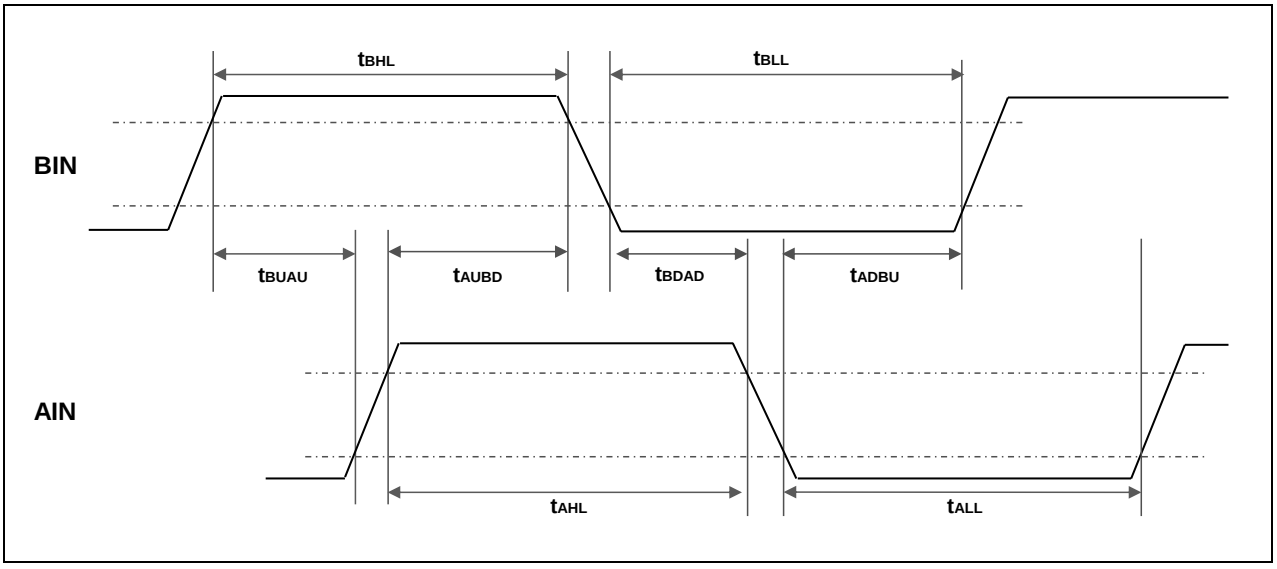
12.4.11 *Quadrature Position/Revolution Counter timing*

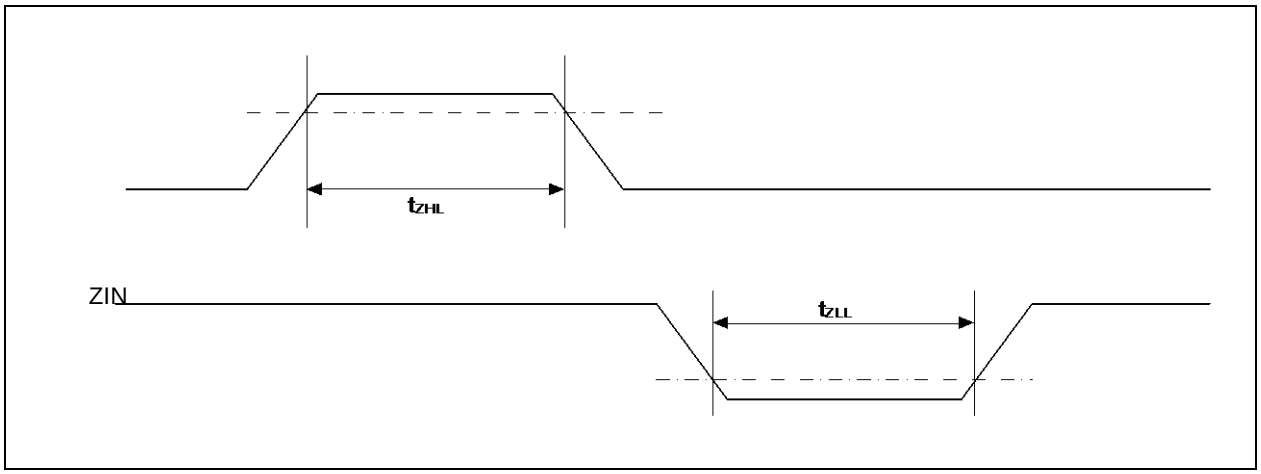
(V_{CC} = 1.65V to 3.6V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

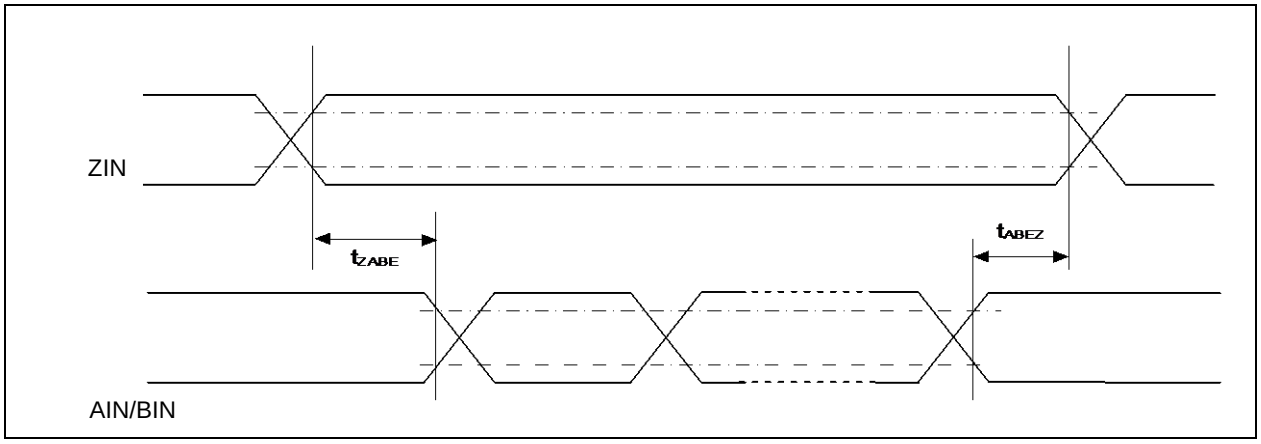
Parameter	Symbol	Conditions	Value		Unit
			Min	Max	
AIN pin H width	t_{AHL}	-	$2t_{CYCP}$[1]	-	ns
AIN pin L width	t_{ALL}	-			
BIN pin H width	t_{BHL}	-			
BIN pin L width	t_{BLL}	-			
BIN rising time from AIN pin H level	t_{AUBU}	PC_Mode2 or PC_Mode3			
AIN falling time from BIN pin H level	t_{BUAD}	PC_Mode2 or PC_Mode3			
BIN falling time from AIN pin L level	t_{ADBD}	PC_Mode2 or PC_Mode3			
AIN rising time from	t_{BDAU}	PC_Mode2 or PC_Mode3			
AIN rising time from BIN pin H level	t_{BUAU}	PC_Mode2 or PC_Mode3			
BIN falling time from AIN pin H level	t_{AUBD}	PC_Mode2 or PC_Mode3			
AIN falling time from BIN pin L level	t_{BDAD}	PC_Mode2 or PC_Mode3			
BIN rising time from AIN pin L level	t_{ADBU}	PC_Mode2 or PC_Mode3			
ZIN pin H width	t_{ZHL}	QCR:CGSC=0			
ZIN pin L width	t_{ZLL}	QCR:CGSC=0			
AIN/BIN rising and falling time from determined ZIN level	t_{ZABE}	QCR:CGSC=1			
Determined ZIN level from AIN/BIN rising and falling time	t_{ABEZ}	QCR:CGSC=1			

[1]. t_{CYCP} indicates the APB bus clock cycle time.About the APB bus number which the Quadrature Position/Revolution Counter is connected to, see Block Diagram in this data sheet.


AIN
BIN
tAHL
tALL
tAUBU
tBUAD
tADBD
tBDAU
tBHL
tBLL


BIN
AIN
tBHL
tBLL
tBUAU
tAUBD
tBDAD
tADBU
tAHL
tALL


tZHL
ZIN
tZLL


ZIN
tZABE
tABEZ
AIN/BIN

12.4.12 *I²C Timing*

(V_{CC} = 1.65V to 3.6V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Conditions	Standard-mode		Fast-mode		Unit	Remarks
			Min	Max	Min	Max		
SCL clock frequency	f_{SCL}	C_L = 30 pF, R = (V_P/I_{OL})[1]	0	100	0	400	kHz	
(Repeated) START condition hold time SDA ↓ → SCL ↓	t_{HDSTA}		4.0	-	0.6	-	µs	
SCL clock L width	t_{LOW}		4.7	-	1.3	-	µs	
SCL clock H width	t_{HIGH}		4.0	-	0.6	-	µs	
(Repeated) START condition setup time SCL ↑ → SDA ↓	t_{SUSTA}		4.7	-	0.6	-	µs	
Data hold time SCL ↓ → SDA ↓ ↑	t_{HDDAT}		0	3.45[2]	0	0.9[3]	µs	
Data setup time SDA ↓ ↑ → SCL ↑	t_{SUDAT}		250	-	100	-	ns	
STOP condition setup time SCL ↑ → SDA ↑	t_{SUSTO}		4.0	-	0.6	-	µs	
Bus free time between STOP condition and START condition	t_{BUF}		4.7	-	1.3	-	µs	
Noise filter	t_{SP}	-	2 t_{CYCP}[4]	-	2 t_{CYCP}[4]	-	ns	

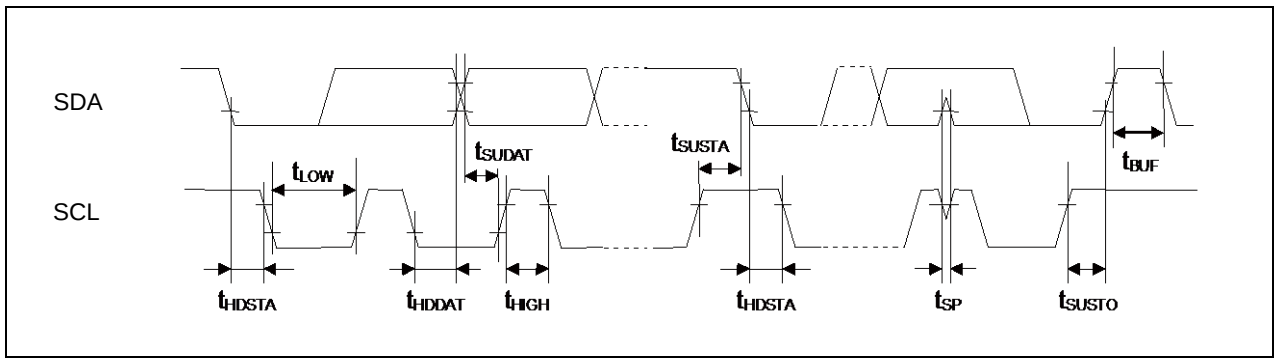
[1]. R and C_L represent the pull-up resistor and load capacitance of the SCL and SDA lines, respectively. V_P indicates the power supply voltage of the pull-up resistor and I_{OL} indicates V_{OL} guaranteed current.

[2]. The maximum t_{HDDAT} must satisfy that it does not extend at least L period (t_{LOW}) of device's SCL signal.

[3]. A Fast-mode I²C bus device can be used on a Standard-mode I²C bus system as long as the device satisfies the requirement of t_{SUDAT} ≥ 250 ns.

[4]. t_{CYCP} is the APB bus clock cycle time. About the APB bus number that I²C is connected to, see Block Diagram in this data sheet.

To use Standard-mode, set the APB bus clock at 2 MHz or more.To use Fast-mode, set the APB bus clock at 8 MHz or more.



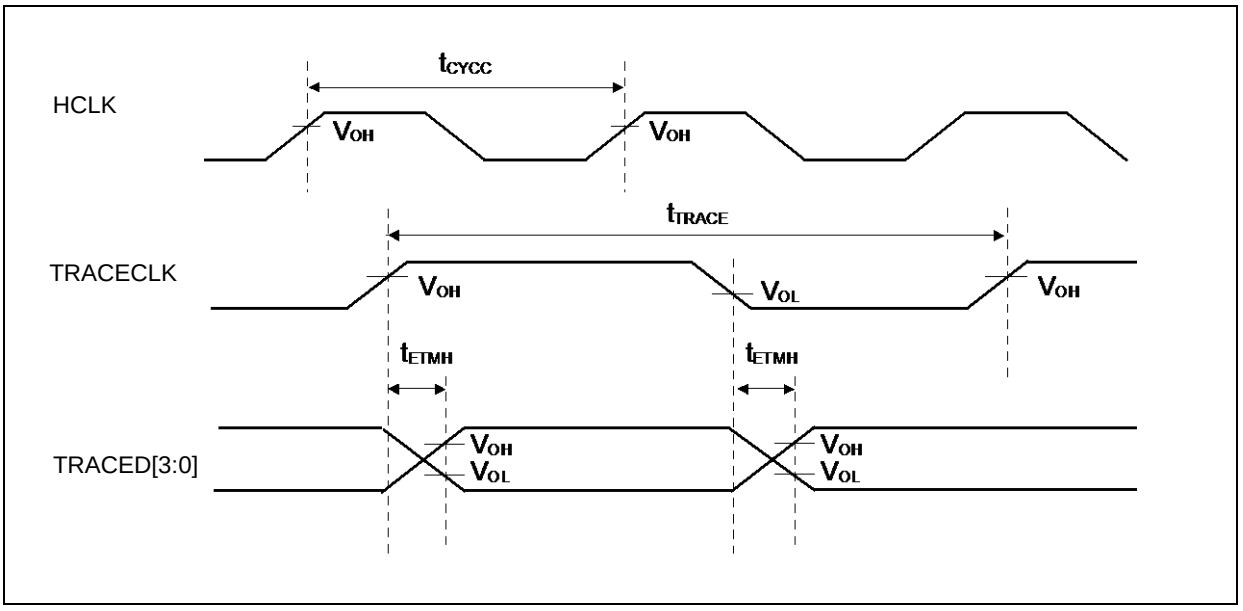
12.4.13 *ETM Timing*

(V_{CC} = 1.65V to 3.6V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Data hold	t_{ETMH}	TRACECLK, TRACED[3:0]	$V_{CC} \geq 2.7V$	2	11	ns	
			$V_{CC} < 2.7V$	2	15		
TRACECLK frequency	1/ t_{TRACE}	TRACECLK	$V_{CC} \geq 2.7V$	-	40	MHz	
			$V_{CC} < 2.7V$	-	20	MHz	
TRACECLK clock cycle	t_{TRACE}		$V_{CC} \geq 2.7V$	25	-	ns	
			$V_{CC} < 2.7V$	50	-	ns	

Note:

- *When the external load capacitance C_L = 30 pF.*



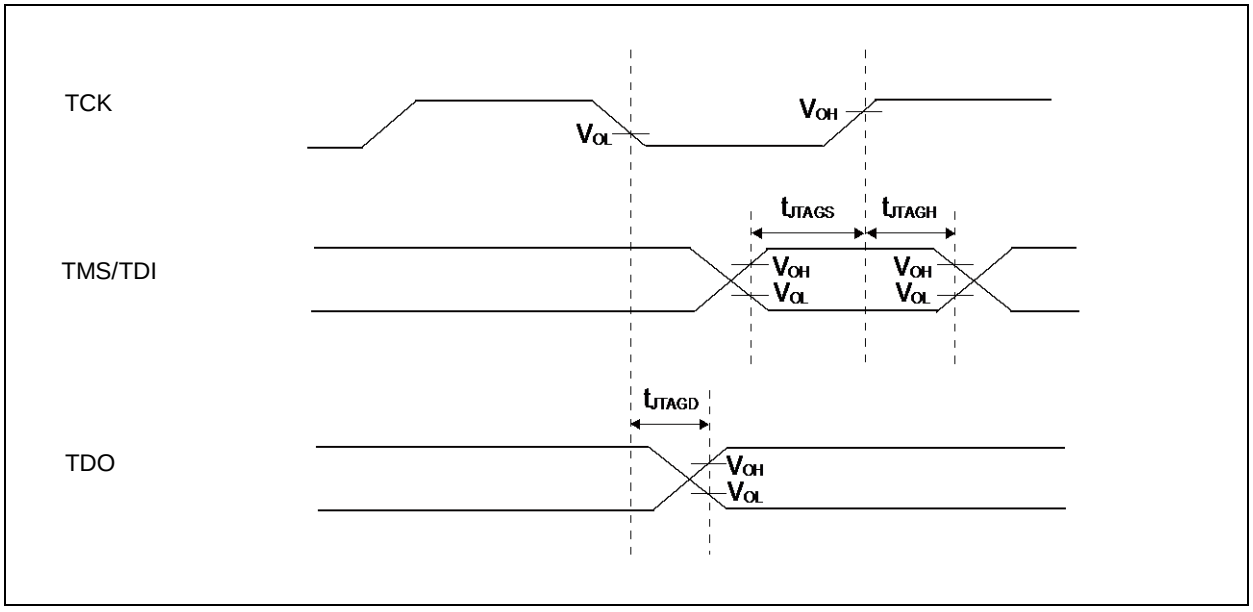
12.4.14 *JTAG Timing*

(V_{CC} = 1.65V to 3.6V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
TMS, TDI setup time	t_{JTAGS}	TCK, TMS, TDI	$V_{CC} \geq 2.7V$	15	-	ns	
			$V_{CC} < 2.7V$				
TMS, TDI hold time	t_{JTAGH}	TCK, TMS, TDI	$V_{CC} \geq 2.7V$	15	-	ns	
			$V_{CC} < 2.7V$				
TDO delay time	t_{JTAGD}	TCK, TDO	$V_{CC} \geq 2.7V$	-	25	ns	
			$V_{CC} < 2.7V$	-	45		

Note:

- *When the external load capacitance C_L = 30 pF.*



12.5 12-bit A/D Converter

12.5.1 *Electrical Characteristics for the A/D Converter*

(V_{CC} = AV_{CC} = 1.65V to 3.6V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	-	-	-	12	bit	
Integral Nonlinearity	-	-	-	± 2.4	± 4.5	LSB	
Differential Nonlinearity	-	-	-	± 2.3	± 2.5	LSB	
Zero transition voltage	V_{ZT}	ANxx	-	± 7	± 15	mV	
Full-scale transition voltage	V_{FST}	ANxx	-	AVRH ± 7	AVRH ± 15	mV	
Conversion time[1]	-	-	2.0	-	-	µs	AV_{CC} ≥ 2.7 V
			4.0	-	-		1.8 V≤ AV_{CC} < 2.7 V
			10	-	-		1.65 V≤ AV_{CC} < 1.8 V
Sampling time[2]	t_S	-	0.6	-	10	us	AV_{CC} ≥ 2.7 V
			1.2	-			1.8 V≤ AV_{CC} < 2.7 V
			3.0	-			1.65 V≤ AV_{CC} < 1.8 V
Compare clock cycle[3]	t_{CCK}	-	100	-	1000	ns	AV_{CC} ≥ 2.7 V
			200				1.8 V≤ AV_{CC} < 2.7 V
			500				1.65 V≤ AV_{CC} < 1.8 V
State transition time to operation permission	t_{STT}	-	-	-	1.0	µs	
Analog input capacity	C_{AIN}	-	-	-	9.4	pF	
Analog input resistor	R_{AIN}	-	-	-	2.2	kΩ	AV_{CC} ≥ 2.7 V
					5.5		1.8 V≤ AV_{CC} < 2.7 V
					10.5		1.65 V≤ AV_{CC} < 1.8 V
Interchannel disparity	-	-	-	-	4	LSB	
Analog port input leak current	-	ANxx	-	-	5	µA	
Analog input voltage	-	ANxx	AV_{SS}	-	AVRH	V	
Reference voltage	-	AVRH	2.7	-	AV_{CC}	V	AV_{CC} ≥ 2.7 V
			AV_{CC}				AV_{CC} < 2.7 V

[1]. The conversion time is the value of sampling time (t_S) + compare time (t_C).

The condition of the minimum conversion time is the following.

AV_{CC} ≥ 2.7 V, HCLK=40 MHz sampling time: 0.6 µs, compare time: 1.4 µs

1.8 V ≤ AV_{CC} < 2.7 V, HCLK=40 MHz sampling time: 1.2 µs, compare time: 2.8 µs

1.65 V ≤ AV_{CC} < 1.8 V, HCLK=40 MHz sampling time: 3 µs, compare time: 7 µs

Ensure that it satisfies the value of the sampling time (t_S) and compare clock cycle (t_{CCK}).

For setting of the sampling time and compare clock cycle, see Chapter 1-1: A/D Converter in FM3 Family Peripheral Manual. Analog Macro Part.

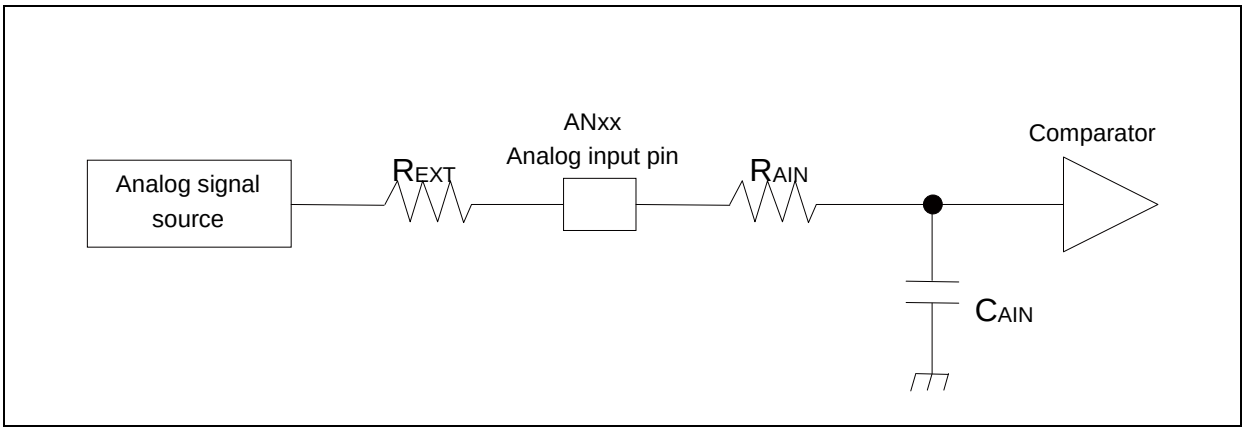
The register settings of the A/D Converter are reflected in the operation according to the APB bus clock timing.

For the number of the APB bus to which the A/D Converter is connected, see Block Diagram. The base clock (HCLK) is used to generate the sampling time and the compare clock cycle.

[2]. A necessary sampling time changes by external impedance.

Ensure that it sets the sampling time to satisfy (Equation 1).

[3]. The compare time (t_C) is the value of (Equation 2).



(Equation 1) $t_S \geq (R_{AIN} + R_{EXT}) \times C_{AIN} \times 9$

t_S: Sampling time[ns]

R_{AIN}: input resistor of A/D[kΩ] = 2.2 kΩ at 2.7 V $\leq AV_{CC} \leq$ 3.6 V

input resistor of A/D[kΩ] = 5.5 kΩ at 1.8 V $\leq AV_{CC} \leq$ 2.7 V

input resistor of A/D[kΩ] = 10.5 kΩ at 1.65 V $\leq AV_{CC} \leq$ 1.8 V

C_{AIN}: input capacity of A/D[pF] = 9.4 pF at 1.65 V $\leq AV_{CC} \leq$ 3.6 V

R_{EXT}: Output impedance of external circuit[kΩ]

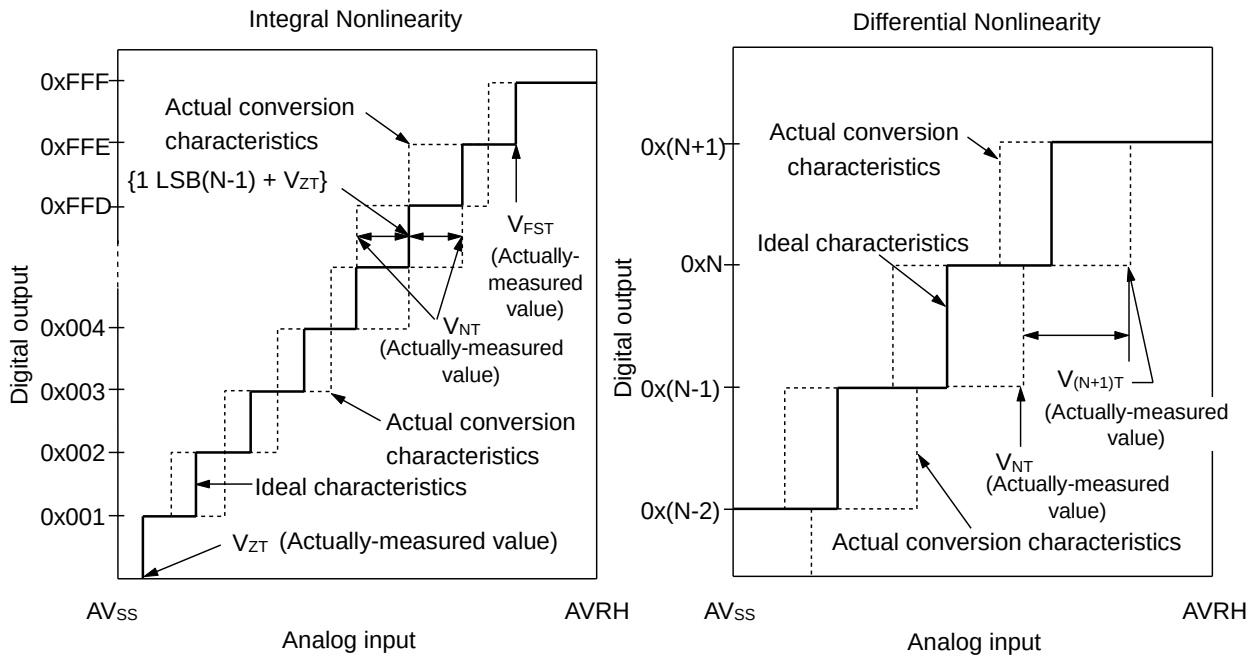
(Equation 2) $t_C = t_{CCK} \times 14$

t_C: Compare time

t_{CCK}: Compare clock cycle

12.5.2 *Definition of 12-bit A/D Converter Terms*

- Resolution: Analog variation that is recognized by an A/D converter.
- Integral Nonlinearity: Deviation of the line between the zero-transition point (0b000000000000 ⟷ 0b000000000001) and the full-scale transition point (0b111111111110 ⟷ 0b111111111111) from the actual conversion characteristics.
- Differential Nonlinearity: Deviation from the ideal value of the input voltage that is required to change the output code by 1 LSB.



$$\text{Integral Nonlinearity of digital output N} = \frac{V_{NT} - \{1LSB \times (N - 1) + V_{ZT}\}}{1LSB} \text{ [LSB]}$$

$$\text{Differential Nonlinearity of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1LSB} - 1 \text{ [LSB]}$$

$$1LSB = \frac{V_{FST} - V_{ZT}}{4094}$$

N: A/D converter digital output value.

V_{ZT}: Voltage at which the digital output changes from 0x000 to 0x001.

V_{FST}: Voltage at which the digital output changes from 0xFFE to 0xFFF.

V_{NT}: Voltage at which the digital output changes from 0x(N − 1) to 0xN.

12.6 Low-Voltage Detection Characteristics

12.6.1 *Low-Voltage Detection Reset*

(T_A = - 40°C to + 85°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detected voltage	VDL	SVHR[1] = 00000	1.38	1.50	1.60	V	When voltage drops
Released voltage	VDH		1.43	1.55	1.65	V	When voltage rises
Detected voltage	VDL	SVHR[1] = 00001	1.43	1.55	1.65	V	When voltage drops
Released voltage	VDH		Same as SVHR = 00000 value			V	When voltage rises
Detected voltage	VDL	SVHR[1] = 00010	1.47	1.60	1.73	V	When voltage drops
Released voltage	VDH		Same as SVHR = 00000 value			V	When voltage rises
Detected voltage	VDL	SVHR[1] = 00011	1.52	1.65	1.78	V	When voltage drops
Released voltage	VDH		Same as SVHR = 00000 value			V	When voltage rises
Detected voltage	VDL	SVHR[1] = 00100	1.56	1.70	1.84	V	When voltage drops
Released voltage	VDH		Same as SVHR = 00000 value			V	When voltage rises
Detected voltage	VDL	SVHR[1] = 00101	1.61	1.75	1.89	V	When voltage drops
Released voltage	VDH		Same as SVHR = 00000 value			V	When voltage rises
Detected voltage	VDL	SVHR[1] = 00110	1.66	1.80	1.94	V	When voltage drops
Released voltage	VDH		Same as SVHR = 00000 value			V	When voltage rises
Detected voltage	VDL	SVHR[1] = 00111	1.70	1.85	2.00	V	When voltage drops
Released voltage	VDH		Same as SVHR = 00000 value			V	When voltage rises
Detected voltage	VDL	SVHR[1] = 01000	1.75	1.90	2.05	V	When voltage drops
Released voltage	VDH		Same as SVHR = 00000 value			V	When voltage rises
Detected voltage	VDL	SVHR[1] = 01001	1.79	1.95	2.11	V	When voltage drops
Released voltage	VDH		Same as SVHR = 00000 value			V	When voltage rises
Detected voltage	VDL	SVHR[1] = 01010	1.84	2.00	2.16	V	When voltage drops
Released voltage	VDH		Same as SVHR = 00000 value			V	When voltage rises
Detected voltage	VDL	SVHR[1] = 01011	1.89	2.05	2.21	V	When voltage drops
Released voltage	VDH		Same as SVHR = 00000 value			V	When voltage rises
Detected voltage	VDL	SVHR[1] = 01100	2.30	2.50	2.70	V	When voltage drops
Released voltage	VDH		Same as SVHR = 00000 value			V	When voltage rises
Detected voltage	VDL	SVHR[1] = 01101	2.39	2.60	2.81	V	When voltage drops
Released voltage	VDH		Same as SVHR = 00000 value			V	When voltage rises
Detected voltage	VDL	SVHR[1] = 01110	2.48	2.70	2.92	V	When voltage drops
Released voltage	VDH		Same as SVHR = 00000 value			V	When voltage rises
Detected voltage	VDL	SVHR[1] = 01111	2.58	2.80	3.02	V	When voltage drops
Released voltage	VDH		Same as SVHR = 00000 value			V	When voltage rises

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detected voltage	VDL	SVHR[1] = 10000	2.67	2.90	3.13	V	When voltage drops
Released voltage	VDH		Same as SVHR = 00000 value			V	When voltage rises
Detected voltage	VDL	SVHR[1] = 10001	2.76	3.00	3.24	V	When voltage drops
Released voltage	VDH		Same as SVHR = 00000 value			V	When voltage rises
Detected voltage	VDL	SVHR[1] = 10010	2.85	3.10	3.35	V	When voltage drops
Released voltage	VDH		Same as SVHR = 00000 value			V	When voltage rises
Detected voltage	VDL	SVHR[1] = 10011	2.94	3.20	3.46	V	When voltage drops
Released voltage	VDH		Same as SVHR = 00000 value			V	When voltage rises
LVD stabilization wait time	t_{LVDW}	-	-	-	5200 × t_{CYCP}[2]	µs	
LVD detection delay time	t_{LVDDL}	-	-	-	200	µs	

[1]. The SVHR bit of Low-Voltage Detection Voltage Control Register (LVD_CTL) is initialized to 00000 by Low-Voltage Detection Reset.

[2]. t_{CYCP} indicates the APB2 bus clock cycle time.

12.6.2 *Interrupt of Low-Voltage Detection*

(T_A = - 40°C to + 85°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detected voltage	VDL	SVHI = 00100	1.56	1.70	1.84	V	When voltage drops
Released voltage	VDH		1.61	1.75	1.89	V	When voltage rises
Detected voltage	VDL	SVHI = 00101	1.61	1.75	1.89	V	When voltage drops
Released voltage	VDH		1.66	1.80	1.94	V	When voltage rises
Detected voltage	VDL	SVHI = 00110	1.66	1.80	1.94	V	When voltage drops
Released voltage	VDH		1.70	1.85	2.00	V	When voltage rises
Detected voltage	VDL	SVHI = 00111	1.70	1.85	2.00	V	When voltage drops
Released voltage	VDH		1.75	1.90	2.05	V	When voltage rises
Detected voltage	VDL	SVHI = 01000	1.75	1.90	2.05	V	When voltage drops
Released voltage	VDH		1.79	1.95	2.11	V	When voltage rises
Detected voltage	VDL	SVHI = 01001	1.79	1.95	2.11	V	When voltage drops
Released voltage	VDH		1.84	2.00	2.16	V	When voltage rises
Detected voltage	VDL	SVHI = 01010	1.84	2.00	2.16	V	When voltage drops
Released voltage	VDH		1.89	2.05	2.21	V	When voltage rises
Detected voltage	VDL	SVHI = 01011	1.89	2.05	2.21	V	When voltage drops
Released voltage	VDH		1.93	2.10	2.27	V	When voltage rises
Detected voltage	VDL	SVHI = 01100	2.30	2.50	2.70	V	When voltage drops
Released voltage	VDH		2.39	2.60	2.81	V	When voltage rises
Detected voltage	VDL	SVHI = 01101	2.39	2.60	2.81	V	When voltage drops
Released voltage	VDH		2.48	2.70	2.92	V	When voltage rises
Detected voltage	VDL	SVHI = 01110	2.48	2.70	2.92	V	When voltage drops
Released voltage	VDH		2.58	2.80	3.02	V	When voltage rises
Detected voltage	VDL	SVHI = 01111	2.58	2.80	3.02	V	When voltage drops
Released voltage	VDH		2.67	2.90	3.13	V	When voltage rises
Detected voltage	VDL	SVHI = 10000	2.67	2.90	3.13	V	When voltage drops
Released voltage	VDH		2.76	3.00	3.24	V	When voltage rises
Detected voltage	VDL	SVHI = 10001	2.76	3.00	3.24	V	When voltage drops
Released voltage	VDH		2.85	3.10	3.35	V	When voltage rises
Detected voltage	VDL	SVHI = 10010	2.85	3.10	3.35	V	When voltage drops
Released voltage	VDH		2.94	3.20	3.46	V	When voltage rises
Detected voltage	VDL	SVHI = 10011	2.94	3.20	3.46	V	When voltage drops
Released voltage	VDH		3.04	3.30	3.56	V	When voltage rises
LVD stabilization wait time	t_{LVDW}	-	-	-	5200 × t_{CYCP}[1]	µs	
LVD detection delay time	t_{LVDDL}	-	-	-	200	µs	

[1]. t_{CYCP} indicates the APB2 bus clock cycle time.

12.7 Flash Memory Write/Erase Characteristics

12.7.1 *Write / Erase time*

(V_{CC} = 1.65V to 3.6V, T_A = - 40°C to + 85°C)

Parameter		Value		Unit	Remarks
		Typ[1]	Max[1]		
Sector erase time	Large Sector	1.1	2.7	s	Includes write time prior to internal erase
	Small Sector	0.3	0.9		
Half word (16-bit) write time		30	528	µs	Not including system-level overhead time
Chip erase time		11.2	30.5	s	Includes write time prior to internal erase

[1].The typical value is immediately after shipment, the maximam value is guarantee value under 100,000 cycle of erase/write.

12.7.2 *Write cycles and data hold time*

Erase/write cycles (cycle)	Data hold time (year)	Remarks
1,000	20[1]	
10,000	10*	

[1]. At average + 85°C

12.8 Return Time from Low-Power Consumption Mode

12.8.1 *Return Factor: Interrupt/WKUP*

The return time from Low-Power consumption mode is indicated as follows. It is from receiving the return factor to starting the program operation.

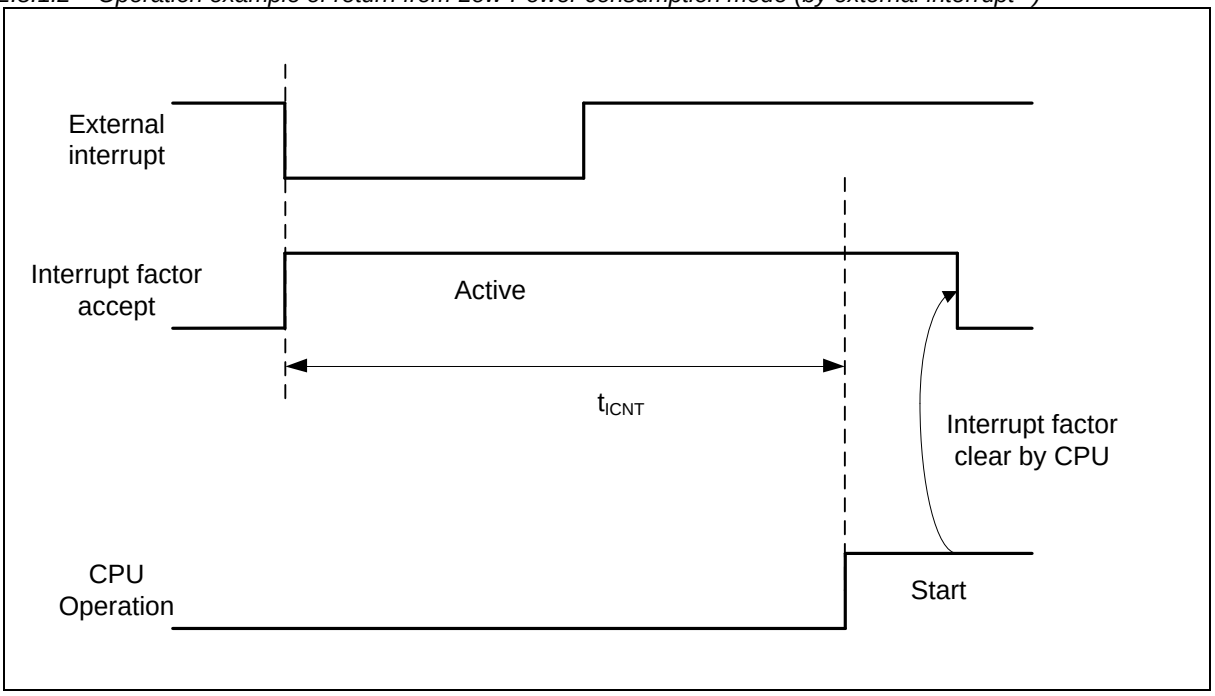
12.8.1.1 Return Count Time

(V_{CC} = 1.65V to 3.6V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Value		Unit	Remarks
		Typ	Max[1]		
Sleep mode	t_{ICNT}	t_{CYCC}		µs	
High-speed CR Timer mode, Main Timer mode, PLL Timer mode		40	80	µs	
Low-speed CR Timer mode		350	700	µs	
Sub Timer mode		690	880	µs	
RTC mode, Stop mode		278	523	µs	
Deep Standby RTC mode		318	603	µs	When RAM is off
Deep Standby Stop mode		278	523	µs	When RAM is on

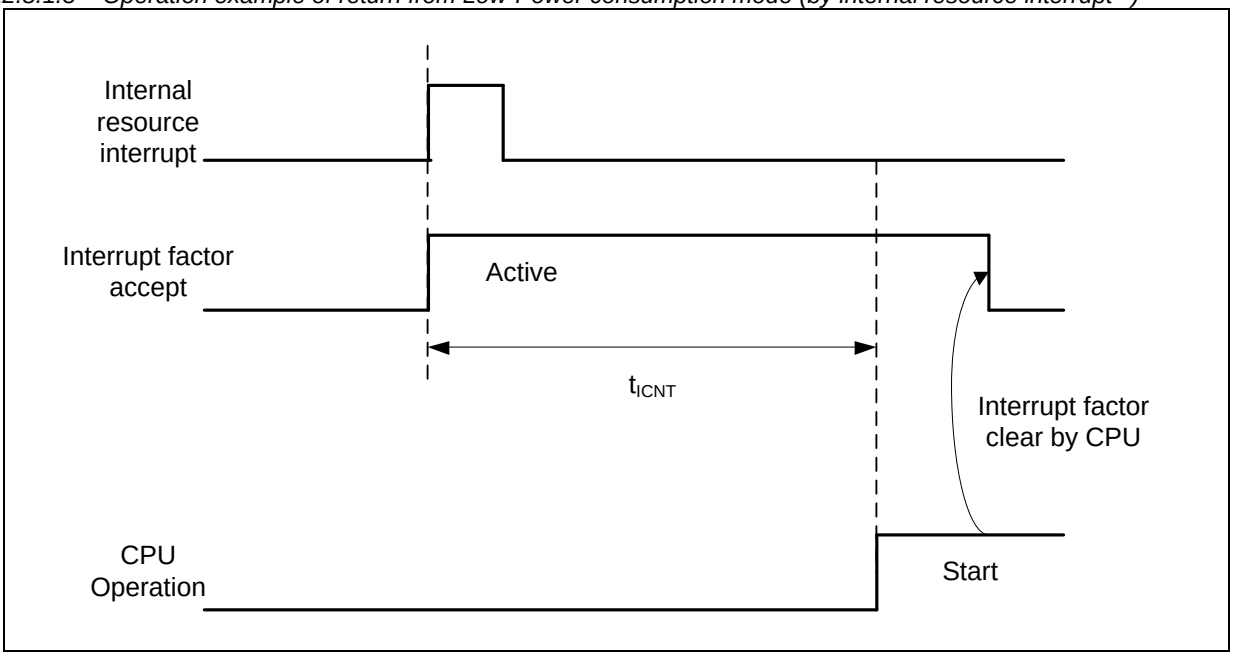
[1]. The maximum value depends on the accuracy of built-in CR.

12.8.1.2 Operation example of return from Low-Power consumption mode (by external interrupt[1])



[1]. External interrupt is set to detecting fall edge.

12.8.1.3 Operation example of return from Low-Power consumption mode (by internal resource interrupt[1])



[1]. Internal resource interrupt is not included in return factor by the kind of Low-Power consumption mode.

Notes:

- *The return factor is different in each Low-Power consumption modes. See Chapter 6: Low Power Consumption Mode and Operations of Standby Modes in FM3 Family Peripheral Manual.*
- *When interrupt recoveries, the operation mode that CPU recoveries depend on the state before the Low-Power consumption mode transition. See Chapter 6: Low Power Consumption Mode in FM3 Family Peripheral Manual.*

12.8.2 *Return Factor: Reset*

The return time from Low-Power consumption mode is indicated as follows. It is from releasing reset to starting the program operation.

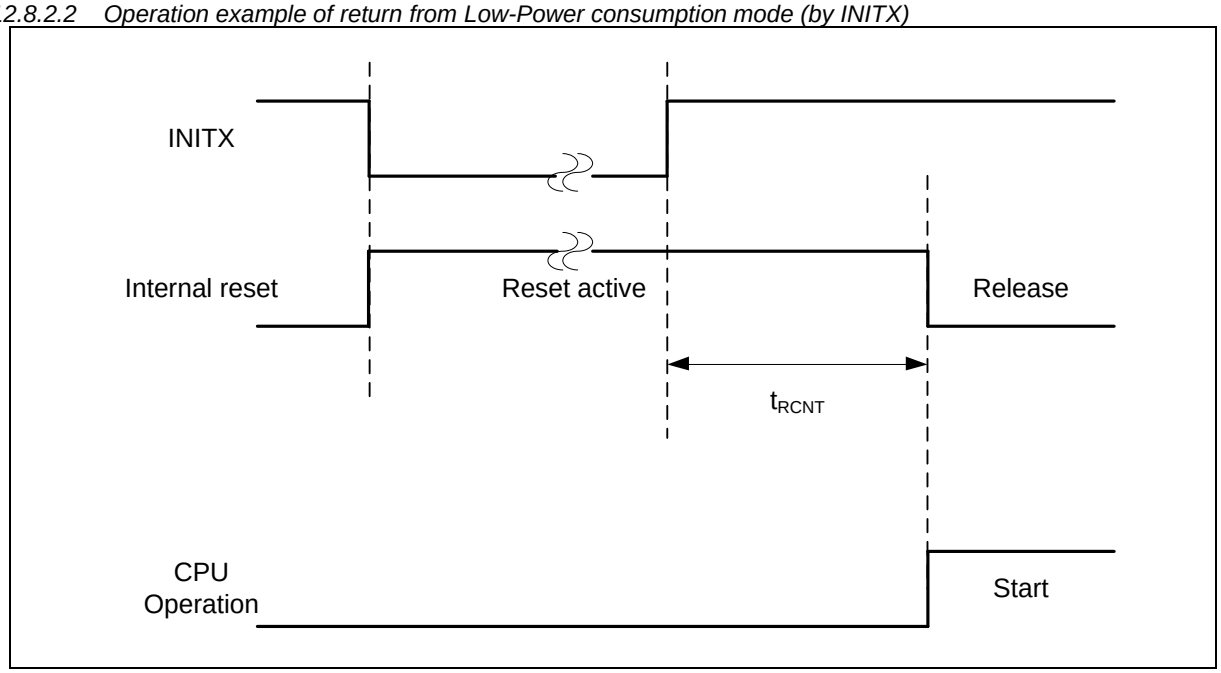
12.8.2.1 Return Count Time

(V_{CC} = 1.65V to 3.6V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

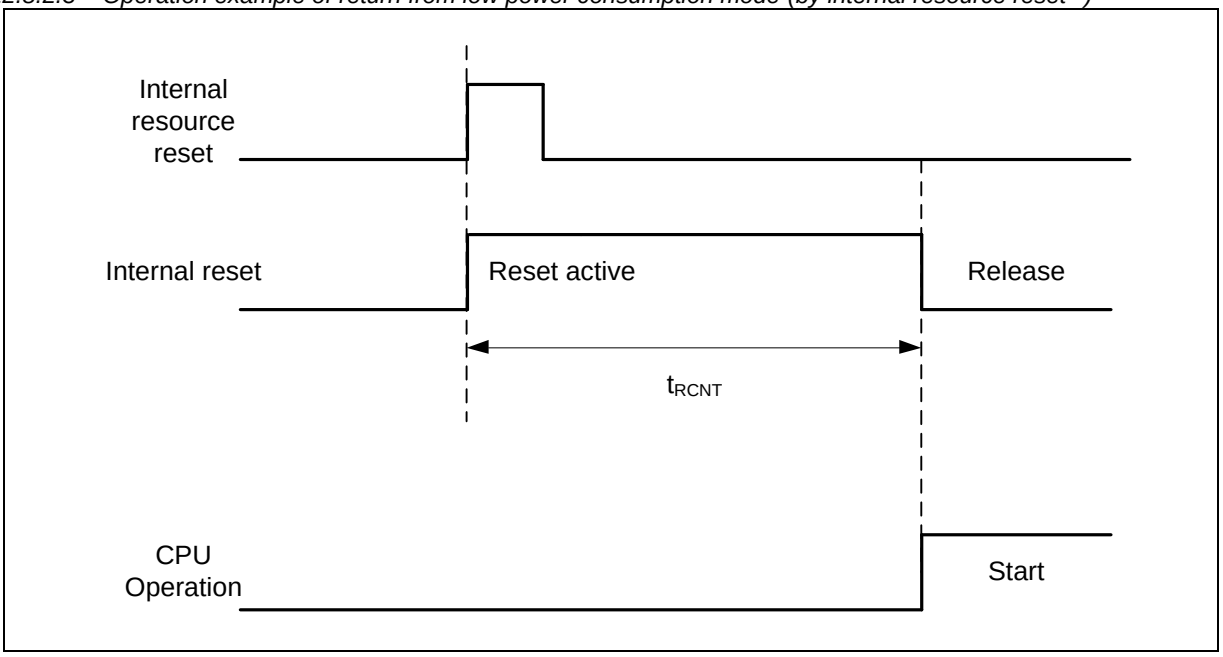
Parameter	Symbol	Value		Unit	Remarks
		Typ	Max[1]		
Sleep mode	t_{RCNT}	148	263	µs	
High-speed CR Timer mode, Main Timer mode, PLL Timer mode		148	263	µs	
Low-speed CR Timer mode		258	483	µs	
Sub Timer mode		322	516	µs	
RTC/Stop mode		278	523	µs	
Deep Standby RTC mode		318	603	µs	When RAM is off
Deep Standby Stop mode		278	523	µs	When RAM is on

[1]. The maximum value depends on the accuracy of built-in CR.

12.8.2.2 Operation example of return from Low-Power consumption mode (by INITX)



12.8.2.3 Operation example of return from low power consumption mode (by internal resource reset[1])



[1]. Internal resource reset is not included in return factor by the kind of Low-Power consumption mode.

Notes:

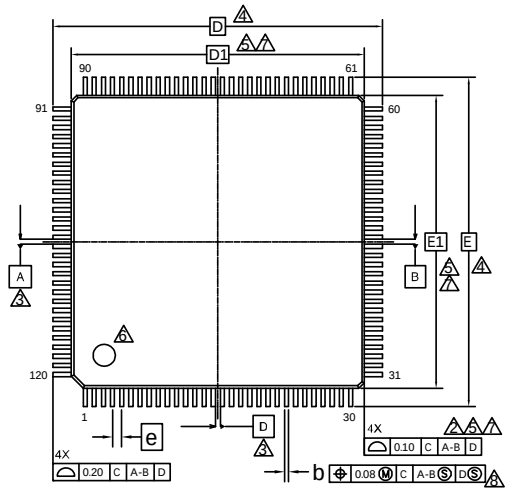
- *The return factor is different in each Low-Power consumption modes. See Chapter 6: Low Power Consumption Mode and Operations of Standby Modes in FM3 Family Peripheral Manual*
- *When interrupt recoveries, the operation mode that CPU recoveries depend on the state before the Low-Power consumption mode transition. See Chapter 6: Low Power Consumption Mode in FM3 Family Peripheral Manual*
- *The time during the power-on reset/low-voltage detection reset is excluded. See 12.4.6 Power-on Reset Timing in 12.4 AC Characteristics in Electrical Characteristics for the detail on the time during the power-on reset/low-voltage detection reset.*
- *When in recovery from reset, CPU changes to the High-speed CR Run mode. When using the main clock or the PLL clock, it is necessary to add the main clock oscillation stabilization wait time or the Main PLL clock stabilization wait time.*
- *The internal resource reset means the watchdog reset and the CSV reset.*

13. Ordering Information

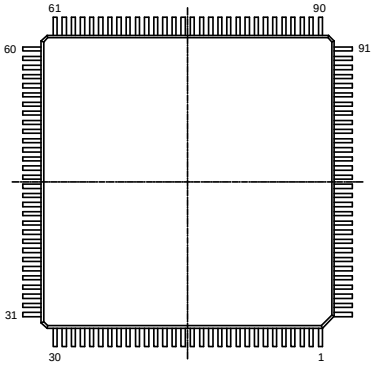
Part number	On-chip Flash memory	On-chip SRAM	Package	Packing
MB9AF154MBPMC-G-JNE2	Main: 256 Kbyte Work: 32 Kbyte	32 Kbyte	Plastic • LQFP 80-pin (0.5 mm pitch), (LQH080)	Tray
MB9AF155MBPMC-G-JNE2	Main: 384 Kbyte Work: 32 Kbyte	48 Kbyte		
MB9AF156MBPMC-G-JNE2	Main: 512 Kbyte Work: 32 Kbyte	64 Kbyte		
MB9AF154MBBGL-GE1	Main: 256 Kbyte Work: 32 Kbyte	32 Kbyte	Plastic • PFBGA 96-pin (0.5 mm pitch), (FDG096)	
MB9AF155MBBGL-GE1	Main: 384 Kbyte Work: 32 Kbyte	48 Kbyte		
MB9AF156MBBGL-GE1	Main: 512 Kbyte Work: 32 Kbyte	64 Kbyte		
MB9AF154NBPMC-G-JNE2	Main: 256 Kbyte Work: 32 Kbyte	32 Kbyte	Plastic • LQFP 100-pin (0.5 mm pitch), (LQI100)	
MB9AF155NBPMC-G-JNE2	Main: 384 Kbyte Work: 32 Kbyte	48 Kbyte		
MB9AF156NBPMC-G-JNE2	Main: 512 Kbyte Work: 32 Kbyte	64 Kbyte		
MB9AF154NBBGL-GE1	Main: 256 Kbyte Work: 32 Kbyte	32 Kbyte	Plastic • PFBGA 112-pin (0.8 mm pitch), (LBC112)	
MB9AF155NBBGL-GE1	Main: 384 Kbyte Work: 32 Kbyte	48 Kbyte		
MB9AF156NBBGL-GE1	Main: 512 Kbyte Work: 32 Kbyte	64 Kbyte		
MB9AF154RBPMC-G-JNE2	Main: 256 Kbyte Work: 32 Kbyte	32 Kbyte	Plastic • LQFP 120-pin (0.5 mm pitch), (LQM120)	
MB9AF155RBPMC-G-JNE2	Main: 384 Kbyte Work: 32 Kbyte	48 Kbyte		
MB9AF156RBPMC-G-JNE2	Main: 512 Kbyte Work: 32 Kbyte	64 Kbyte		

14. Package Dimensions

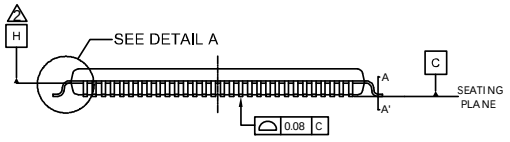
Package Type	Package Code
LQFP 120	LQM120



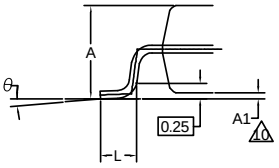
TOP VIEW



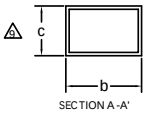
BOTTOM VIEW



SIDE VIEW



DETAIL A



SECTION A-A'

SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.05	—	0.15
b	0.17	0.22	0.27
c	0.115	—	0.195
D	18.00 BSC		
D1	16.00 BSC		
e	0.50 BSC		
E	18.00 BSC		
E1	16.00 BSC		
L	0.45	0.60	0.75
θ	0°	—	8°

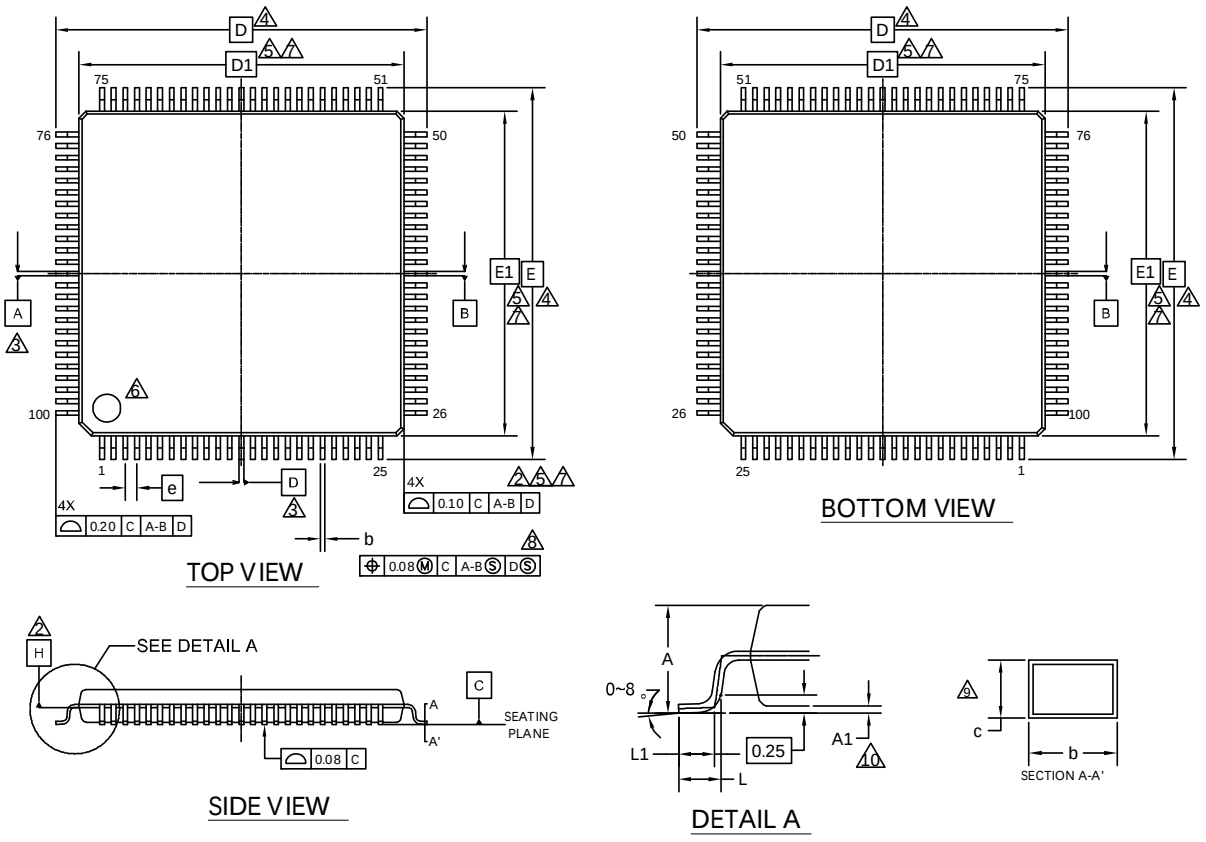
NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
11. JEDEC SPECIFICATION NO. REF: N/A.

002-16172 **

PACKAGE OUTLINE, 120 LEAD LQFP
18.0X18.0X1.7 MM LQM120 REV**

Package Type	Package Code
LQFP 100	LQI100



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.05	—	0.15
b	0.15	—	0.27
c	0.09	—	0.20
D	16.00 BSC		
D1	14.00 BSC		
e	0.50 BSC		
E	16.00 BSC		
E1	14.00 BSC		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70

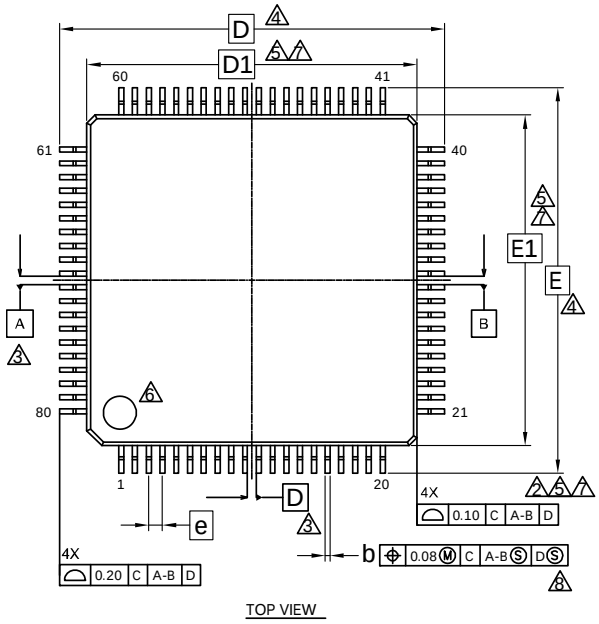
NOTES :

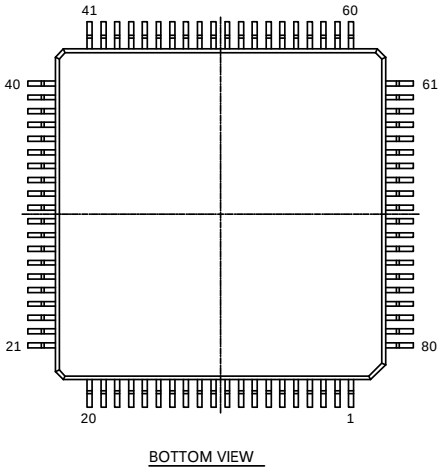
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

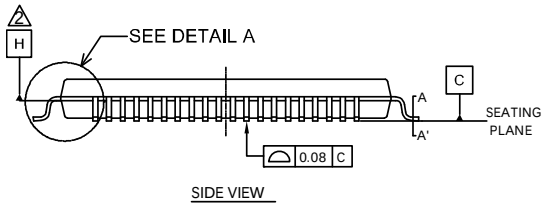
002-11500 *A

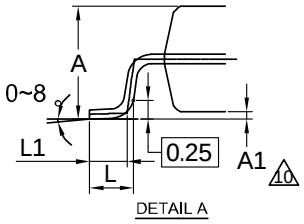
PACKAGE OUTLINE, 100 LEAD LQFP
14.0X14.0X1.7 MM LQI100 REV*A

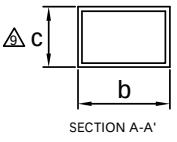
Package Type	Package Code
LQFP 80	LQH080











SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.05	—	0.15
b	0.15	—	0.27
c	0.09	—	0.20
D	14.00 BSC.		
D1	12.00 BSC.		
e	0.50 BSC		
E	14.00 BSC.		
E1	12.00 BSC.		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70

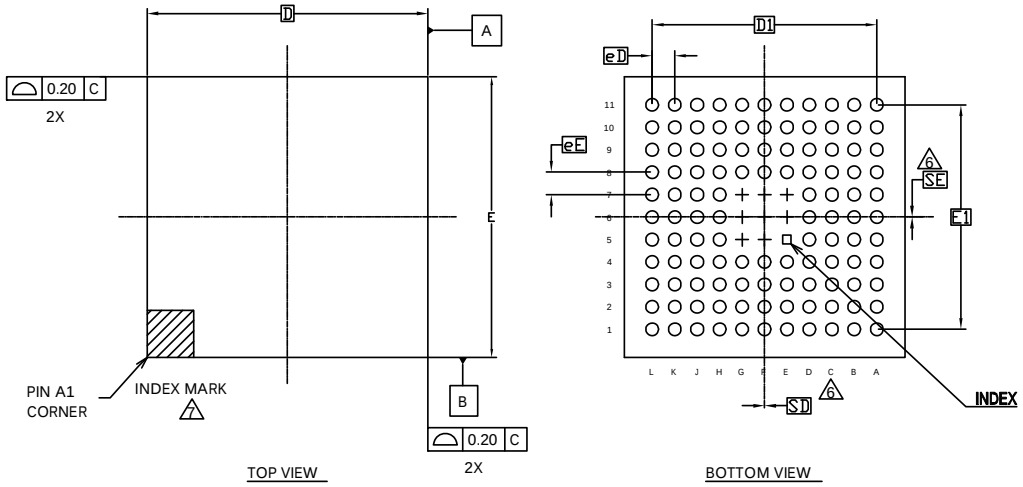
NOTES

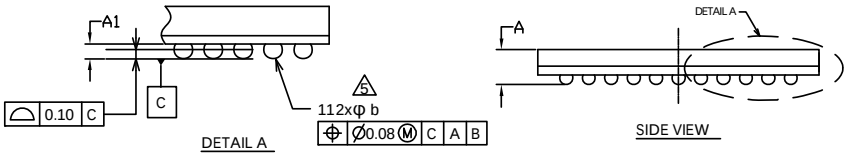
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (mm)
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-11501 **

PACKAGE OUTLINE, 80 LEAD LQFP
12.0X12.0X1.7 MM LQH080 Rev **

Package Type	Package Code
BGA 112	LBC112





SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	-	-	1.45
A1	0.25	0.35	0.45
D		10.00 BSC	
E		10.00 BSC	
D1		8.00 BSC	
E1		8.00 BSC	
MD		11	
ME		11	
N		112	
Ø b	0.35	0.45	0.55
eD		0.80 BSC	
eE		0.80 BSC	
SD		0.00	
SE		0.00	

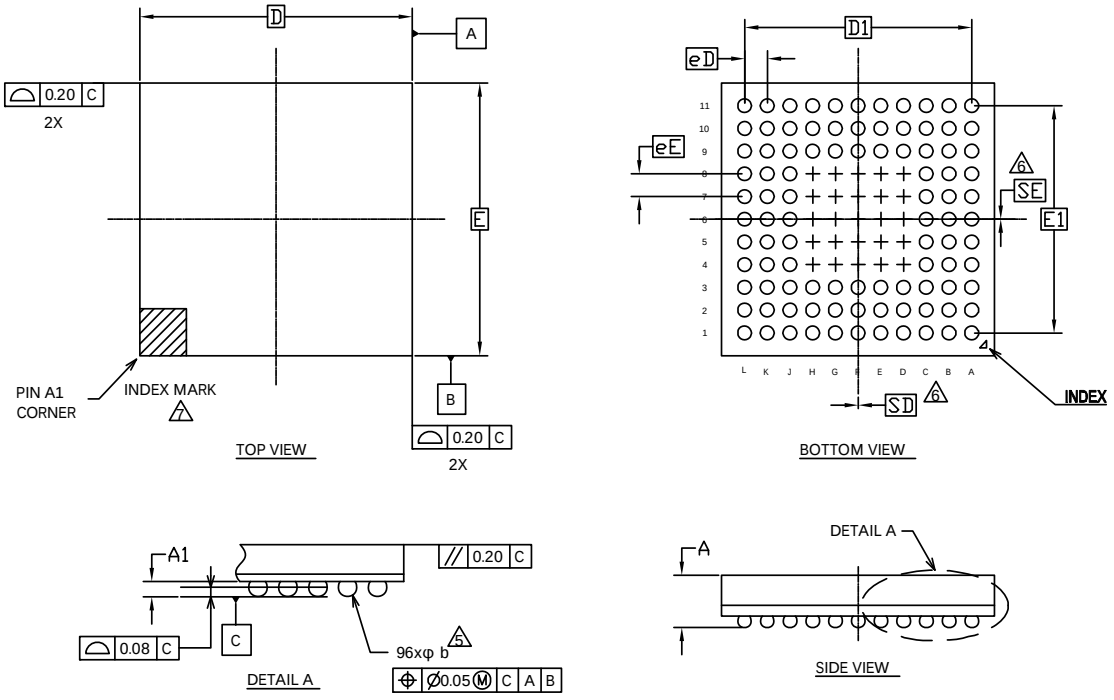
NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. SOLDER BALL POSITION DESIGNATIO N PER JEP95, SECTION 3, SPP-020.
3. "e" REPRESENTS THE SOLDER BALL GRID PITCH.
4. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
5. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
6. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" OR "SE" = 0.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
7. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK METALIZED MARK, INDENTATION OR OTHER MEANS.
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED SOLDER BALLS.

002-13225 **

PACKAGE OUTLINE, 112 BALL FBGA
10.00X10.00X1.45 MM LBC112 REV**

Package Type	Package Code
BGA 96	FDG096



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	-	-	1.30
A1	0.15	0.25	0.35
D		6.00 BSC	
E		6.00 BSC	
D1		5.00 BSC	
E1		5.00 BSC	
MD		11	
ME		11	
N		96	
Ø b	0.20	0.30	0.40
eD		0.50 BSC	
eE		0.50 BSC	
SD		0.00	
SE		0.00	

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. SOLDER BALL POSITION DESIGNATIO N PER JEP95, SECTION 3, SPP-020.
3. "e" REPRESENTS THE SOLDER BALL GRID PITCH.
4. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
5. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
6. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" OR "SE" = 0.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
7. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK METALIZED MARK, INDENTATION OR OTHER MEANS.
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED SOLDER BALLS.

002-13224 **

PACKAGE OUTLINE, 96 BALL FBGA
6.0X6.0X1.3 MM FDG096 REV**

15. Errata

This chapter describes the errata for MB9B150R series. Details include errata trigger conditions, scope of impact, available workaround, and silicon revision applicability.

Contact your local Cypress Sales Representative if you have questions.

15.1 Part Numbers Affected

Part Number
Initial Revision
MB9AF154RPMC-G-JNE2, MB9AF155RPMC-G-JNE2, MB9AF156RPMC-G-JNE2, MB9AF154NPMC-G-JNE2, MB9AF155NPMC-G-JNE2, MB9AF156NPMC-G-JNE2, MB9AF154NBGL-GE1, MB9AF155NBGL-GE1, MB9AF156NBGL-GE1, MB9AF154MPMC-G-JNE2, MB9AF155MPMC-G-JNE2, MB9AF156MPMC-G-JNE2, MB9AF154MBGL-GE1, MB9AF155MBGL-GE1, MB9AF156MBGL-GE1
Rev. A
MB9AF154RAPMC-G-JNE2, MB9AF155RAPMC-G-JNE2, MB9AF156RAPMC-G-JNE2, MB9AF154NAPMC-G-JNE2, MB9AF155NAPMC-G-JNE2, MB9AF156NAPMC-G-JNE2, MB9AF154NABGL-GE1, MB9AF155NABGL-GE1, MB9AF156NABGL-GE1, MB9AF154MAPMC-G-JNE2, MB9AF155MAPMC-G-JNE2, MB9AF156MAPMC-G-JNE2, MB9AF154MABGL-GE1, MB9AF155MABGL-GE1, MB9AF156MABGL-GE1

15.2 Qualification Status

Product Status: In Production − Qual.

15.3 Errata Summary

This table defines the errata applicability to available devices.

Items	Part Number	Silicon Revision	Fix Status
[1] HDMI-CEC arbitration lost issue	Refer to 15.1	Initial rev.	Fixed in Rev. A
[2] HDMI-CEC polling message issue	Refer to 15.1	Initial rev., Rev. A	Fixed in Rev. B

1. HDMI-CEC arbitration lost issue

■ PROBLEM DEFINITION
Large external load on CEC bus may cause arbitration lost.

■ PARAMETERS AFFECTED
N/A

■ TRIGGER CONDITION(S)
The arbitration lost detection mechanism samples outputting signals and determines that arbitration lost occurs if sampled signals do not match the outputting signals. The large external load on the CEC bus increases slew rate of the signals. The increased slew

rate makes the mismatch between outputting signals and sampled signals and the mismatch misleads MCU that arbitration lost occurs.

■ SCOPE OF IMPACT
Once the arbitration lost is detected, the CEC aborts the transmission. Any transmission cannot be completed.

■ WORKAROUND
This error cannot be avoided by any software. Reduce the external load.

■ FIX STATUS
This issue was fixed in Rev. A.

2. HDMI-CEC polling message issue

■ PROBLEM DEFINITION
Error#1) While MCU sends a Polling Message, it always returns a NACK to a message coming to the MCU from another node.

Error#2) MCU always waits for 7-bit signal free on CEC line before it drives the line even when the last line initiator was another node.

■ PARAMETERS AFFECTED
N/A

■ TRIGGER CONDITION(S)
This error always happens.

■ SCOPE OF IMPACT
MCU does not reply properly to another node.

■ WORKAROUND
The software workaround is applied to Error #1.

1. Store 0x0 to SFREE register.
2. Monitor CEC line with GPIO and wait until High on the CEC line lasts for the signal free time.
3. Store frame data to TXDATA register and store 0x0F to RCADR1 or RCADR2 register.

It sends a message after 3~4 clocks of 32.768 kHz clock when TXDATA is stored.

If the device receives a frame from another node within 2~3 clocks after storing TXDATA, the bus error occurs and if the device receives a frame from another node within 3~4 clocks after storing TXDATA, the arbitration lost occurs. In these cases:

4-A-1. Set RCADR1 or RCADR2 to former value from 0x0F to reply ACK

4-A-2. Return back to step 2 above

If the device receives a frame from another node within 1~2 clocks after storing TXDATA, take these steps.

4-B-1. Monitor CEC line with GPIO after 50us from storing TXDATA

4-B-2. Set TXEN to 1 -> 0 -> 1 immediately when GPIO finds Low on the CEC line

4-B-3. Set RCADR1 or RCADR2 to former value from 0x0F to reply ACK

4-B-4. Return back to step 2 above

For Error #2, there is no software workaround, but signal free time of fixed 7-bit does not violate HDMI-CEC specification. The specification says signal free time must be more than and equals to 5-bit.

■ FIX STATUS
■ This issue was fixed in Rev. B.

16. Major Changes

Spansion Publication Number: MB9A150RB_DS706-00047

Page	Section	Change Results
Revision 0.1		
-	-	Initial release
Revision 1.0		
-	-	Preliminary → Data Sheet
1	Features On-chip Memories	Corrected the description of "Flash memory".
7	1. Product Lineup 1.2. Function	Corrected the value of channel number of the "Base Timer".
71	7.Handling Devices	■ Added the description of "Crystal oscillator circuit". ■ Added the description of "Sub crystal oscillator".
74	8.Block Diagram	Corrected the figure. ■ TIOA: input → input/output ■ TIOB: output → input
75	10.Memory Map 10.1 Memory Map (1)	Corrected the value of address of "SRAM0".
75	10.2 Memory Map (2)	Added the footnote.
78, 79	11. Pin Status In Each CPU State 11.1 List of Pin Status	■ Corrected the Return from Deep standby mode state of "Pin status type H". ■ Corrected the functon group of "Pin status type I".
77, 78	13. Electrical Characteristics 13.3. DC Characteristics 13.3.1 Current Rating	■ Revised the value of "TBD". ■ Revised the typical value of "Power supply voltage (I_{CCH}, I_{CCT}, I_{CCR})". ■ Added the "Flash Memory Write/Erase current ($I_{CCFLASH}$)". ■ Added the footnote.
94, 95,	13.4. AC Characteristics 13.4.2 Sub Clock Input Characteristics	■ Added the description of Note of "Input frequency (F_{CL})". ■ Added the footnote.
	13.4.3 Built-in CR Oscillation Characteristics 13.4.3.1 Built-in high-speed CR	■ Reviced the condition. ■ Corrected the value. ■ Added the item of "Frequency stabilization time". ■ Added the footnote.
99	13.4.7. External Bus Timing 13.4.7.1. Separate Bus Access Asynchronous SRAM Mode	■ Corrected the value. ■ Deleted the "MWEX ↓ → Data output time". ■ Added the "MCSX ↓ → Data output time". ■ Corrected the figure.
101	13.4.7.2 Separate Bus Access Synchronous SRAM Mode	■ Corrected the "MCLK↑ → Data output time". ■ Added the "MCLK↑ → Data hold time". ■ Corrected the figure.
110, 112, 114, 116	13.4.9. CSIO Timming	Corrected the description of section title. UART Timming → CSIO Timming
		Corrected the description of "Note". UART is connected → Multi-function Serial is connected
122	13.4.12 I^2C Timing	Added the footnote.
125	13.5. 12-bit A/D Converter	■ Revised the parameter. ■ Revised the symbol. ■ Corrected the value.

Page	Section	Change Results
127	13.5.2 Definition of 12-bit A/D Converter Terms	■ Revised the parameter. ■ Revised the symbol.
128, 129	13.6. Low-Voltage Detection Characteristics 13.6.1 Low-Voltage Detection Reset	■ Corrected "Conditions" and "Value" in the table. ■ Added the Item. ■ Added the footnote.
130	13.6.2 Interrupt of Low-Voltage Detection	Added the Item.
Revision 1.1		
-	-	Company name and layout design change
Revision 2.0		
-	-	Corrected the Series name. MB9A150R Series → MB9A150RA Series
-	-	Corrected the Product name as follows. MB9AF156MA, MB9AF155MA, MB9AF154MA MB9AF156NA, MB9AF155NA, MB9AF154NA MB9AF156RA, MB9AF155RA, MB9AF154RA
1	Features External Bus Interface	Added the Item. ■ Maximum area size : Up to 256 Mbytes
1	Multi-function Serial Interface	Corrected the description of "I^2C"
2	Multi-function Timer	Corrected the channel count of "A/D activation compare"
7	1.Product Lineup 1.2 Function	Added the footnote
9	2. Packages	Delete the following packages. ■ FPT-100P-M36 ■ FPT-80P-M40
11	3. Pin Assignment 3.2 FPT-100P-M36	Delete the Item
12	3.3 FPT-80P-M37	Corrected the description of section title. FPT-80P-M37/M40 →FPT-80P-M37
15 – 36	4. List Of Pin Function 4.1 List of numbers	Delete column of terminal number "QFP-100"
37 - 60	4.2 List of pin functions	Delete column of terminal number "QFP-100"
75	10.Memory Map 10.1 Memory Map (1)	Corrected the address "External Device Area"
88	13.Electrical Characteristics 13.2.Recommended Operating Conditions	Add the footnote
89	13.3.DC Characteristics 13.3.1 Current rating	■ Corrected the Condition ■ Delete the minmun value ■ Corrected the remarks ■ Add the footnote
116	13.9. CSIO Timing 13.9.4 Synchronous serial (SPI=1, SCINV=1)	Corrected the figure of "MS bit=1"
117	13.9 CSIO Timing 13.4.9.5. External clock(EXT=1):asyntironous only	Corrected the figure

Page	Section	Change Results
118	13.4.10. External Input Timing	Add the terminal as follows ■ FRCKx ■ ICxx ■ DTTIxX
122	13.4.12. I^2C Timing	Corrected the description as follows. ■ Typical mode → Standard-mode ■ High-speed mode → Fast-mode
125	13.5.12-bit A/D Converter 13.5.1 Electrical Characteristics for the A/D Converter	■ Corrected the terminal name AN00 to AN23 → ANxx ■ Corrected the minmum value of "Sampling time" ■ Corrected the max and min value of "State transition time to oprerationpermission" ■ Corrected the footnote
137	14. ORDERING INFORMATON	Corrected the "Part number"
Revision 3.0		
-	-	Corrected the Series name. MB9A150RA Series → MB9A150RB Series
-	-	Corrected the Product name as follows. MB9AF156MB, MB9AF155MB, MB9AF154MB MB9AF156NB, MB9AF155NB, MB9AF154NB MB9AF156RB, MB9AF155RB, MB9AF154RB
76	10.Memory Map 10.2. Memory map(2)	Added the summary of Flash memory sector
89	13. Electrical Characteristics 13.3. DC Characteristics 13.3.1 Current rating	■ Changed the table format ■ Added Main TIMER mode current ■ Moved A/D Converter Current
96	13. Electrical Characteristics 13.4. AC Characteristics 13.4.1 Operating Conditions of Main PLL 13.4.2 Operating Conditions of Main PLL	■ Added the figure of Main PLL connection
97	13. Electrical Characteristics 13. 4. AC Characteristics 13.4.6. Power-on Reset Timing	■ Added Time until releasing Power-on reset ■ Changed the figure of timing
110 - 117	13.Electrical Characteristics 13.4. AC Characteristics 13.4.9 CSIO/UART Timing	■ Modified from UART Timing to CSIO/UART Timing ■ Changed from Internal shift clock operation to Master mode ■ Changed from External shift clock operation to Slave mode
125	13. Electrical Characteristics 13.5. 12bit A/D Converter	■ Added the typical value of Integral Nonlinearity, Differential Nonlinearity, Zero transition voltage and Full-scale transition voltage ■ Added the value of conversion time at AV_{CC} < 2.7 V
132 - 134	13. Electrical Characteristics 13.8. Return Time from Low-Power Consumption Mode	Added Return Time from Low-Power Consumption Mode
137	14. Ordering Information	Changed notation of part number
137 - 141	15. Package Dimensions	Deleted FPT-100P-M36 and FPT-80P-M40

NOTE: Please see "Document History" about later revised information.

Document History

Document Title: MB9A150RB Series 32-bit ARM® Cortex®-M3 FM3 Microcontroller
Document Number: 002-05646

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	–	AKIH	04/28/2015	Migrated to Cypress and assigned document number 002-05646. No change to document contents or format.
*A	5226742	AKIH	04/27/2016	Updated to Cypress template
*B	5535819	YSKA	02/09/2017	Updated “12.4.6 Power-On Reset Timing”. Changed parameter from “Power Supply rise time(Tr)[ms]” to “Power ramp rate(dV/dt)[mV/us]” and added some comments (Page 96) Modified RTC description in “Features, Real-Time Clock(RTC)” as below Changed starting count value from 01 to 00. Deleted “second , or day of the week” in the Interrupt function (Page 3) Added Notes for JTAG (Page 59), Changed “J-TAG” to” JTAG” in “4.2 List of Pin Functions” (Page 40) Updated Package code and dimensions as follows (Page 8-13, 135-140) FPT-80P-M37 -> LQH080, BGA-96P-M07 -> FDG096, FPT-100P-M23 -> LQI100, BGA-112P-M04 -> LBC112, FPT-120P-M37 -> LQM120 Added “15.Errta (Page 141)” Deleted the note below from the footer of the first page. "CONFIDENTIAL - RELEASED ONLY UNDER NONDISCLOSURE AGREEMENT (NDA)" (Page 1) Added the Baud rate spec in “12.4.9 CSIO/UART Timing”(Page 109, 111, 113, 115)
*C	5774754	YSAT	06/19/2017	Adapted new Cypress logo

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