

## Automotive fully integrated H-bridge motor driver

Datasheet - production data



### Features

Type	$R_{DS(on)}$	$I_{out}$	$V_{CCmax}$
VNH5019A-E	18 mΩ typ (per leg)	30 A	41 V

- AEC-Q100 qualified
- ECOPACK®: lead free and RoHS compliant
- Output current: 30 A
- 3 V CMOS compatible inputs
- Undervoltage and overvoltage shutdown
- High-side and low-side thermal shutdown
- Cross-conduction protection
- Current limitation
- Very low standby power consumption
- PWM operation up to 20 kHz
- Protection against:
  - Loss of ground and loss of  $V_{CC}$
  - Current sense output proportional to motor current
  - Charge pump output for reverse polarity protection
  - Output protected against short to ground and short to  $V_{CC}$



monolithic high-side drivers and two low-side switches. The high-side driver switch is designed using STMicroelectronics' well known and proven proprietary VIPower® M0 technology that allows to efficiently integrate on the same die a true Power MOSFET with an intelligent signal/protection circuit.

The three dice are assembled in a MultiPowerSO-30 package on electrically isolated lead-frames. This package, specifically designed for harsh automotive environments offers improved thermal performance thanks to exposed die pads. The input signals  $IN_A$  and  $IN_B$  can directly interface to the microcontroller to select the motor direction and the brake condition.

The  $DIAG_A/EN_A$  or  $DIAG_B/EN_B$ , when connected to an external pull-up resistor, enable one leg of the bridge. They also provide a feedback digital diagnostic signal. The CS pin allows to monitor the motor current by delivering a current proportional to its value when CS\_DIS pin is driven low or left open. The PWM, up to 20 KHz, lets us to control the speed of the motor in all possible conditions. In all cases, a low-level state on the PWM pin turns off both the  $LS_A$  and  $LS_B$  switches. When PWM rises to a high-level,  $LS_A$  or  $LS_B$  turn-on again depending on the input pin state. Output current limitation and thermal shutdown protects the concerned high-side in short to ground condition.

The short to battery condition is revealed by the overload detector or by thermal shutdown that latches off the relevant low-side.

Active  $V_{CC}$  pin voltage clamp protects the device against low energy spikes in all configurations for the motor. The CP pin provides the necessary gate drive for an external N-channel PowerMOS used for reverse polarity protection.

### Description

The VNH5019A-E is a full bridge motor driver intended for a wide range of automotive applications. The device incorporates a dual

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# 1 Block diagram and pin description

Figure 1. Block diagram

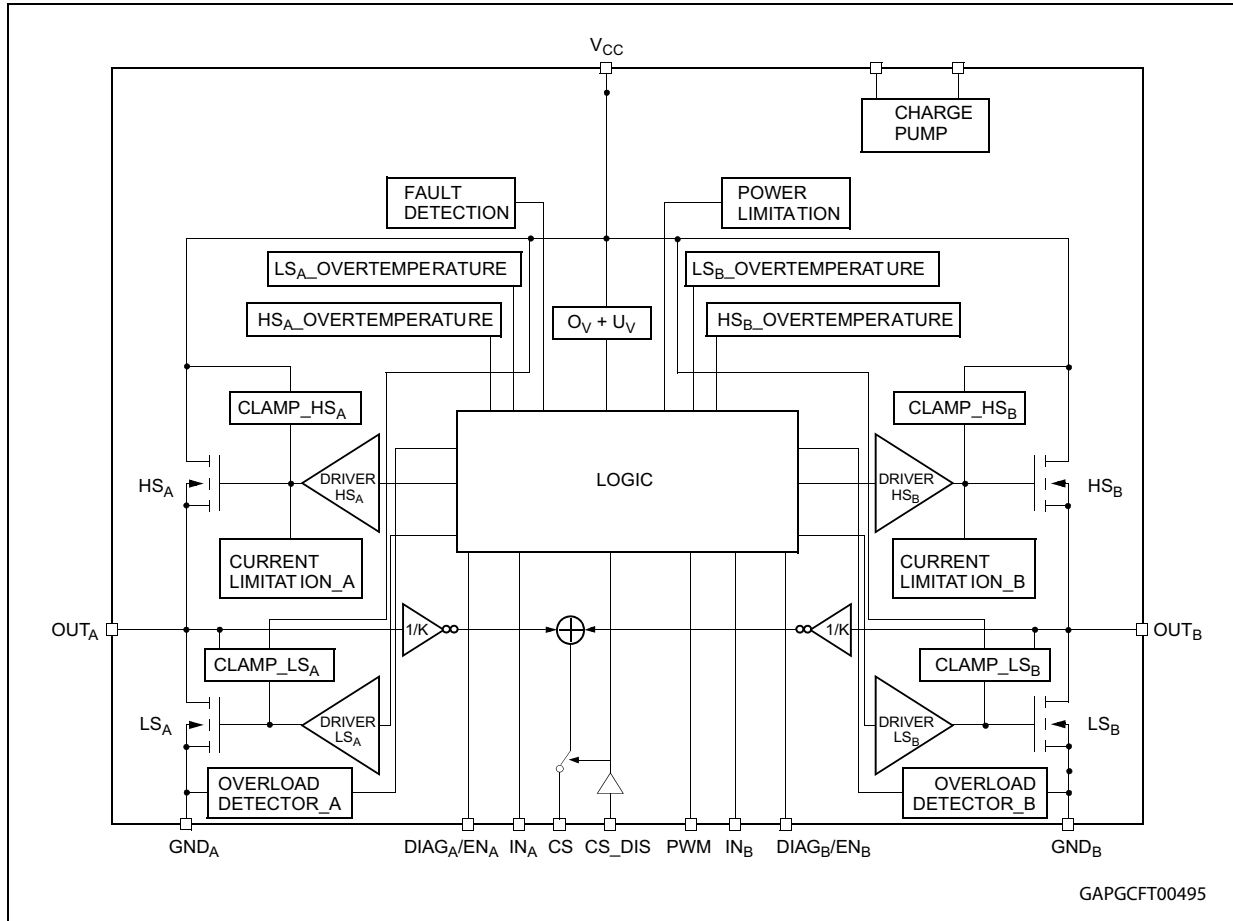


Figure 2. Configuration diagram (top view)

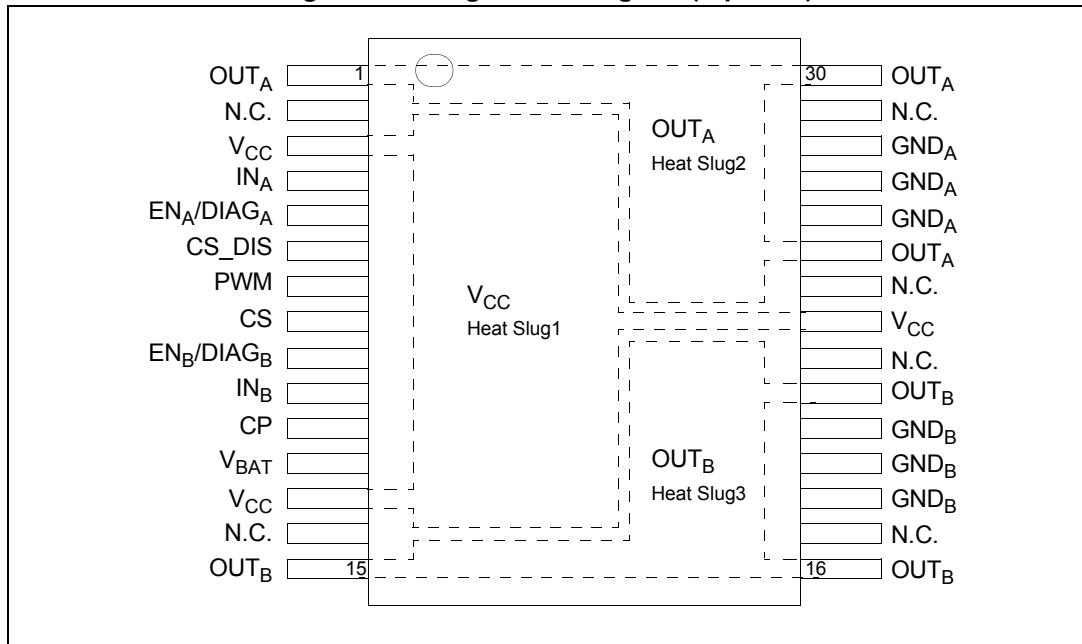


Table 1. Suggested connections for unused and non connected pins

Connection / pin	Current sense	N.C.	OUTx	INPUTx, PWM DIAGx/ENx CS_DIS
Floating	Not allowed	X	X	X
To ground	Through 1 kΩ resistor	X	Not allowed	Through 10 kΩ resistor

Table 2. Pin definitions and functions

Pin	Symbol	Function
1, 25, 30	OUT <sub>A</sub> , Heat Slug2	Source of high-side switch A / drain of low-side switch A, power connection to the motor
2,14,17, 22, 24,29	N.C.	Not connected
3, 13, 23	V <sub>CC</sub> , Heat Slug1	Drain of high-side switches and connection to the drain of the external PowerMOS used for the reverse battery protection
12	V <sub>BAT</sub>	Battery connection and connection to the source of the external PowerMOS used for the reverse battery protection
5	EN <sub>A</sub> /DIAG <sub>A</sub>	Status of high-side and low-side switches A; open drain output. This pin must be connected to an external pull-up resistor. When externally pulled low, it disables half-bridge A. In case of fault detection (thermal shutdown of a high-side FET or excessive ON-state voltage drop across a low-side FET), this pin is pulled low by the device (see <a href="#">Table 13: Truth table in fault conditions (detected on OUT<sub>A</sub>)</a> ).

**Table 2. Pin definitions and functions (continued)**

Pin	Symbol	Function
6	CS_DIS	Active high CMOS compatible pin to disable the current sense pin
4	IN <sub>A</sub>	Clockwise input. CMOS compatible
7	PWM	PWM input. CMOS compatible.
8	CS	Output of current sense. This output delivers a current proportional to the motor current, if CS_DIS is low or left open. The information can be read back as an analog voltage across an external resistor.
9	EN <sub>B</sub> /DIAG <sub>B</sub>	Status of high-side and low-side switches B; Open drain output. This pin must be connected to an external pull up resistor. When externally pulled low, it disables half-bridge B. In case of fault detection (thermal shutdown of a high-side FET or excessive ON-state voltage drop across a low-side FET), this pin is pulled low by the device (see <a href="#">Table 13: Truth table in fault conditions (detected on OUTA)</a> ).
10	IN <sub>B</sub>	Counter clockwise input. CMOS compatible
11	CP	Connection to the gate of the external MOS used for the reverse battery protection
15, 16, 21	OUT <sub>B</sub> , Heat Slug3	Source of high-side switch B / drain of low-side switch B, power connection to the motor
26, 27, 28	GND <sub>A</sub>	Source of low-side switch A and power ground <sup>(1)</sup>
18, 19, 20	GND <sub>B</sub>	Source of low-side switch B and power ground <sup>(1)</sup>

1. GNDA and GNDB must be externally connected together

**Table 3. Block descriptions<sup>(1)</sup>**

Name	Description
Logic control	Allows the turn-on and the turn-off of the high-side and the low-side switches according to the <a href="#">Table 12</a> .
Oversvoltage + undervoltage	Shut down the device outside the range [4.5 V to 24 V] for the battery voltage.
High-side, low-side and clamp voltage	Protect the high-side and the low-side switches from the high-voltage on the battery line in all configuration for the motor.
High-side and low-side driver	Drive the gate of the concerned switch to allow a proper R <sub>DS(on)</sub> for the leg of the bridge.
Linear current limiter	Limits the motor current, by reducing the high-side switch gate-source voltage when short-circuit to ground occurs.
High-side and low-side overtemperature protection	In case of short-circuit with the increase of the junction temperature, it shuts down the concerned driver to prevent its degradation and to protect the die.
Low-side overload detector	Detects when low-side current exceeds shutdown current and latches off the concerned low-side.

**Table 3. Block descriptions<sup>(1)</sup> (continued)**

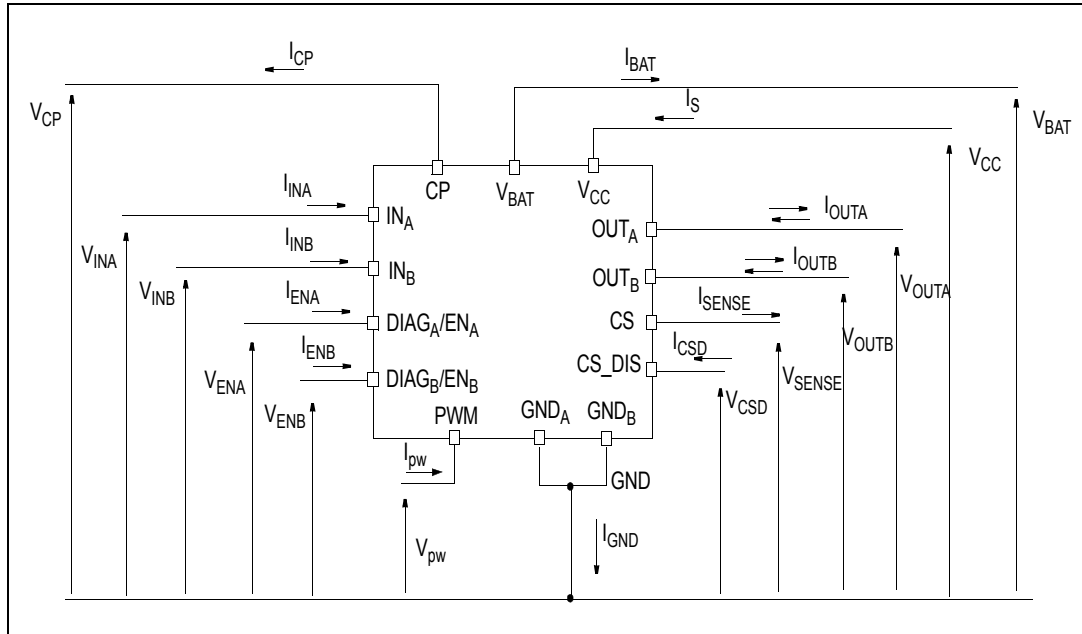
Name	Description
Charge pump	Provides the voltage necessary to drive the gate of the external PowerMOS used for the reverse polarity protection
Fault detection	Signalizes an abnormal condition of the switch (output shorted to ground or output shorted to battery) by pulling down the concerned ENx/DIAGx pin.
Power limitation	Limits the power dissipation of the high-side driver inside safe range in case of short to ground condition.

1. See [Figure 1](#)



## 2 Electrical specifications

Figure 3. Current and voltage conventions



### 2.1 Absolute maximum ratings

Stressing the device above the rating listed in the “absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE program and other relevant quality document.

Table 4. Absolute maximum rating

Symbol	Parameter	Value	Unit
V <sub>BAT</sub>	Maximum battery voltage <sup>(1)</sup>	-16	V
		+41	V
V <sub>CC</sub>	Maximum bridge supply voltage	+ 41	V
I <sub>max</sub>	Maximum output current (continuous)	30	A
I <sub>R</sub>	Reverse output current (continuous)	-30	A
I <sub>IN</sub>	Input current (IN <sub>A</sub> and IN <sub>B</sub> pins)	+/- 10	mA
I <sub>EN</sub>	Enable input current (DIAG <sub>A</sub> /EN <sub>A</sub> and DIAG <sub>B</sub> /EN <sub>B</sub> pins)	+/- 10	mA
I <sub>pw</sub>	PWM input current	+/- 10	mA
I <sub>CP</sub>	CP output current	+/- 10	mA
I <sub>CS_DIS</sub>	CS_DIS input current	+/- 10	mA

Table 4. Absolute maximum rating (continued)

Symbol	Parameter	Value	Unit
$V_{CS}$	Current sense maximum voltage	$V_{CC} - 41$	V
		$+V_{CC}$	V
$V_{ESD}$	Electrostatic discharge (human body model: R = 1.5 k $\Omega$ , C = 100 pF)	2	kV
$T_c$	Case operating temperature	-40 to 150	$^{\circ}$ C
$T_{STG}$	Storage temperature	-55 to 150	$^{\circ}$ C

1. This applies with the n-channel MOSFET used for the reverse battery protection. Otherwise  $V_{BAT}$  has to be shorted to  $V_{CC}$ .

## 2.2 Thermal data

Table 5. Thermal data

Symbol	Parameter	Max. value	Unit
$R_{thj-case}$	Thermal resistance junction-case HSD	1.7	$^{\circ}$ C/W
	Thermal resistance junction-case LSD	3.2	$^{\circ}$ C/W
$R_{thj-amb}$	Thermal resistance junction-ambient	See <a href="#">Figure 18</a>	$^{\circ}$ C/W

### 2.3 Electrical characteristics

Values specified in this section are for  $8\text{ V} < V_{CC} < 21\text{ V}$ ,  $-40\text{ °C} < T_j < 150\text{ °C}$ , unless otherwise specified.

**Table 6. Power section**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{CC}$	Operating bridge supply voltage		5.5		24	V
$I_S$	Supply current	OFF-state with all fault cleared and $EN_x = 0\text{ V}$ (standby): $I_{N_A} = I_{N_B} = PWM = 0$ ; $T_j = 25\text{ °C}$ ; $V_{CC} = 13\text{ V}$ $I_{N_A} = I_{N_B} = PWM = 0$ OFF-state (no standby): $I_{N_A} = I_{N_B} = PWM = 0$ ; $EN_x = 5\text{ V}$		10	15 60	$\mu\text{A}$ $\mu\text{A}$
		ON-state: $I_{N_A}$ or $I_{N_B} = 5\text{ V}$ , no PWM $I_{N_A}$ or $I_{N_B} = 5\text{ V}$ , PWM = 20 kHz		4	8 8	$\text{mA}$ $\text{mA}$
$R_{ONHS}$	Static high-side resistance	$I_{OUT} = 15\text{ A}$ ; $T_j = 25\text{ °C}$		12.0		$\text{m}\Omega$
		$I_{OUT} = 15\text{ A}$ ; $T_j = -40\text{ °C}$ to $150\text{ °C}$			26.5	
$R_{ONLS}$	Static low-side resistance	$I_{OUT} = 15\text{ A}$ ; $T_j = 25\text{ °C}$		6.0		$\text{m}\Omega$
		$I_{OUT} = 15\text{ A}$ ; $T_j = -40\text{ °C}$ to $150\text{ °C}$			11.5	
$V_f$	High-side free-wheeling diode forward voltage	$I_f = 15\text{ A}$ , $T_j = 150\text{ °C}$		0.6	0.8	V
$I_{L(off)}$	High-side OFF-state output current (per channel)	$T_j = 25\text{ °C}$ ; $V_{OUTX} = EN_x = 0\text{ V}$ ; $V_{CC} = 13\text{ V}$			3	$\mu\text{A}$
		$T_j = 125\text{ °C}$ ; $V_{OUTX} = EN_x = 0\text{ V}$ ; $V_{CC} = 13\text{ V}$			5	

**Table 7. Logic inputs ( $I_{N_A}$ ,  $I_{N_B}$ ,  $EN_A$ ,  $EN_B$ , PWM, CS\_DIS)**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{IL}$	Low-level input voltage	Normal operation ( $DIAG_x/EN_x$ pin acts as an input pin)			0.9	V
$V_{IH}$	High-level input voltage	Normal operation ( $DIAG_x/EN_x$ pin acts as an input pin)	2.1			V
$I_{INL}$	Low-level input current	$V_{IN} = 0.9\text{ V}$	1			$\mu\text{A}$
$I_{INH}$	High-level input current	$V_{IN} = 2.1\text{ V}$			10	$\mu\text{A}$
$V_{IHYST}$	Input hysteresis voltage	Normal operation ( $DIAG_x/EN_x$ pin acts as an input pin)	0.15			V

Table 7. Logic inputs (IN<sub>A</sub>, IN<sub>B</sub>, EN<sub>A</sub>, EN<sub>B</sub>, PWM, CS\_DIS) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V <sub>ICL</sub>	Input clamp voltage	I <sub>IN</sub> = 1 mA	5.5	6.3	7.5	V
		I <sub>IN</sub> = -1 mA	-1.0	-0.7	-0.3	
V <sub>DIAG</sub>	Enable low-level output voltage	Fault operation (DIAG <sub>X</sub> /EN <sub>X</sub> pin acts as an output pin); I <sub>EN</sub> = 1 mA			0.4	V

Table 8. Switching (V<sub>CC</sub> = 13 V, R<sub>LOAD</sub> = 0.87 Ω, T<sub>j</sub> = 25 °C)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
f	PWM frequency		0		20	kHz
t <sub>d(on)</sub>	HSD rise time	Input rise time < 1 μs (see Figure 9)			250	μs
t <sub>d(off)</sub>	HSD fall time	Input rise time < 1 μs (see Figure 9)			250	μs
t <sub>r</sub>	LSD rise time	(see Figure 8)		1	2	μs
t <sub>f</sub>	LSD fall time	(see Figure 8)		1	2	μs
t <sub>DEL</sub>	Delay time during change of operating mode	(see Figure 7)	200	400	1600	μs
t <sub>rr</sub>	High-side free wheeling diode reverse recovery time	(see Figure 10)		110		ns
I <sub>RM</sub>	Dynamic cross-conduction current	I <sub>OUT</sub> = 15 A (see Figure 10)		2		A

Table 9. Protection and diagnostic

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V <sub>USD</sub>	V <sub>CC</sub> undervoltage shutdown			4.5	5.5	V
V <sub>USDhyst</sub>	V <sub>CC</sub> undervoltage shutdown hysteresis			0.5		V
V <sub>OV</sub>	V <sub>CC</sub> overvoltage shutdown		24	27	30	V
I <sub>LIM_H</sub>	High-side current limitation		30	50	70	A
I <sub>SD_LS</sub>	Low-side shutdown current		70	115	160	A
V <sub>CLPHS</sub> <sup>(1)</sup>	High-side clamp voltage (V <sub>CC</sub> to OUT <sub>A</sub> = 0 or OUT <sub>B</sub> = 0)	I <sub>OUT</sub> = 15 A	43	48	54	V
V <sub>CLPLS</sub> <sup>(1)</sup>	Low-side clamp voltage (OUT <sub>A</sub> = V <sub>CC</sub> or OUT <sub>B</sub> = V <sub>CC</sub> to GND)	I <sub>OUT</sub> = 15 A	27	30	33	V
T <sub>TSD</sub> <sup>(2)</sup>	Thermal shutdown temperature	V <sub>IN</sub> = 2.1 V	150	175	200	°C

**Table 9. Protection and diagnostic (continued)**

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
T <sub>TSD_LS</sub>	Low-side thermal shutdown temperature	V <sub>IN</sub> = 0 V	150	175	200	°C
T <sub>TR</sub> <sup>(3)</sup>	Thermal reset temperature		135			°C
T <sub>HYST</sub> <sup>(3)</sup>	Thermal hysteresis		7	15		°C

1. The device is able to pass the ESD and ISO pulse requirements as specified in the [Table 15](#).
2. T<sub>TSD</sub> is the minimum threshold temperature between HS and LS
3. Valid for both HSD and LSD

**Table 10. Current sense (8 V < V<sub>CC</sub> < 21 V)**

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
K <sub>0</sub>	I <sub>OUT</sub> /I <sub>SENSE</sub>	I <sub>OUT</sub> = 3 A, V <sub>SENSE</sub> = 0.5 V, T <sub>j</sub> = -40 °C to 150 °C	4670	7110	10110	
dK <sub>0</sub> /K <sub>0</sub>	Analog current sense ratio drift	I <sub>OUT</sub> = 3 A; V <sub>SENSE</sub> = 0.5 V, T <sub>j</sub> = -40 °C to 150 °C	-19		19	%
K <sub>1</sub>	I <sub>OUT</sub> /I <sub>SENSE</sub>	I <sub>OUT</sub> = 8 A, V <sub>SENSE</sub> = 1.3V, T <sub>j</sub> = -40 °C to 150 °C	6060	7030	8330	
dK <sub>1</sub> /K <sub>1</sub>	Analog current sense ratio drift	I <sub>OUT</sub> = 8 A; V <sub>SENSE</sub> = 1.3V, T <sub>j</sub> = -40 °C to 150 °C	-14		14	%
K <sub>2</sub>	I <sub>OUT</sub> /I <sub>SENSE</sub>	I <sub>OUT</sub> = 15 A, V <sub>SENSE</sub> = 2.4 V, T <sub>j</sub> = -40 °C to 150 °C	6070	6990	7810	
dK <sub>2</sub> /K <sub>2</sub>	Analog current sense ratio drift	I <sub>OUT</sub> = 15 A; V <sub>SENSE</sub> = 2.4 V, T <sub>j</sub> = -40 °C to 150 °C	-12		12	%
K <sub>3</sub>	I <sub>OUT</sub> /I <sub>SENSE</sub>	I <sub>OUT</sub> = 25 A, V <sub>SENSE</sub> = 4 V, T <sub>j</sub> = -40 °C to 150 °C	6000	6940	7650	
dK <sub>3</sub> /K <sub>3</sub>	Analog current sense ratio drift	I <sub>OUT</sub> = 25 A; V <sub>SENSE</sub> = 4 V, T <sub>j</sub> = -40 °C to 150 °C	-12		12	%
V <sub>SENSE</sub>	Max analog sense output voltage	I <sub>OUT</sub> = 15 A, R <sub>SENSE</sub> = 1.1 kΩ	5			V
I <sub>SENSE0</sub>	Analog sense leakage current	I <sub>OUT</sub> = 0 A, V <sub>SENSE</sub> = 0 V, V <sub>CSD</sub> = 5 V, V <sub>IN</sub> = 0 V, T <sub>j</sub> = -40 to 150 °C	0		5	μA
		I <sub>OUT</sub> = 0 A, V <sub>SENSE</sub> = 0 V, V <sub>CSD</sub> = 0 V, V <sub>IN</sub> = 5 V, T <sub>j</sub> = -40 to 150 °C	0		100	
t <sub>DSENSEH</sub>	Delay response time from falling edge of CS_DIS pin	V <sub>IN</sub> = 5 V, V <sub>SENSE</sub> < 4 V, I <sub>OUT</sub> = 8 A, I <sub>SENSE</sub> = 90% of I <sub>SENSEmax</sub> (see fig <a href="#">Figure 13</a> )			50	μs
t <sub>DSENSEL</sub>	Delay response time from rising edge of CS_DIS pin	V <sub>IN</sub> = 5 V, V <sub>SENSE</sub> < 4 V, I <sub>OUT</sub> = 8 A, I <sub>SENSE</sub> = 10% of I <sub>SENSEmax</sub> (see fig <a href="#">Figure 13</a> )			20	μs

Table 11. Charge pump

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V <sub>CP</sub>	Charge pump output voltage	EN <sub>X</sub> = 5 V	V <sub>CC</sub> + 5		V <sub>CC</sub> + 10	V
		EN <sub>X</sub> = 5 V, V <sub>CC</sub> = 4.5 V		10.5		
I <sub>BAT</sub>	Charge pump standby current	EN <sub>A</sub> = EN <sub>B</sub> = 0 V		200		nA

## 2.4 Waveforms and truth table

In normal operating conditions the DIAG<sub>X</sub>/EN<sub>X</sub> pin is considered as an input pin by the device. This pin must be externally pulled-high

PWM pin usage: in all cases, a “0” on the PWM pin turns-off both LS<sub>A</sub> and LS<sub>B</sub> switches. When PWM rises back to “1”, LS<sub>A</sub> or LS<sub>B</sub> turn-on again depending on the input pin state.

Table 12. Truth table in normal operating conditions

IN <sub>A</sub>	IN <sub>B</sub>	DIAG <sub>A</sub> /EN <sub>A</sub>	DIAG <sub>B</sub> /EN <sub>B</sub>	OUT <sub>A</sub>	OUT <sub>B</sub>	CS (V <sub>CSD</sub> = 0 V)	Operating mode
1	1	1	1	H	H	High imp.	Brake to V <sub>CC</sub>
1	0	1	1	H	L	I <sub>SENSE</sub> = I <sub>OUT</sub> /K	Clockwise (CW)
0	1	1	1	L	H	I <sub>SENSE</sub> = I <sub>OUT</sub> /K	Counterclockwise (CCW)
0	0	1	1	L	L	High imp.	Brake to GND

Figure 4. Typical application circuit for DC to 20 kHz PWM operation with reverse battery protection (option A)

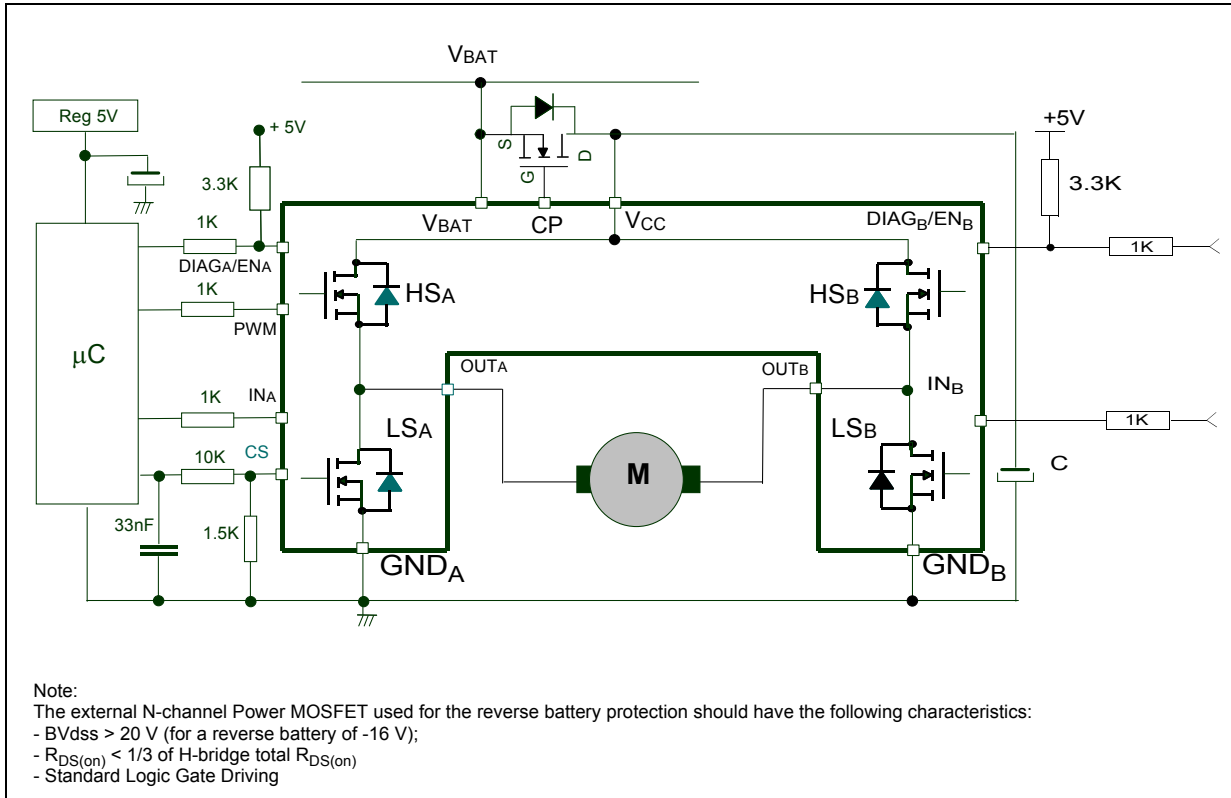


Figure 5. Typical application circuit for DC to 20 kHz PWM operation with reverse battery protection (option B)

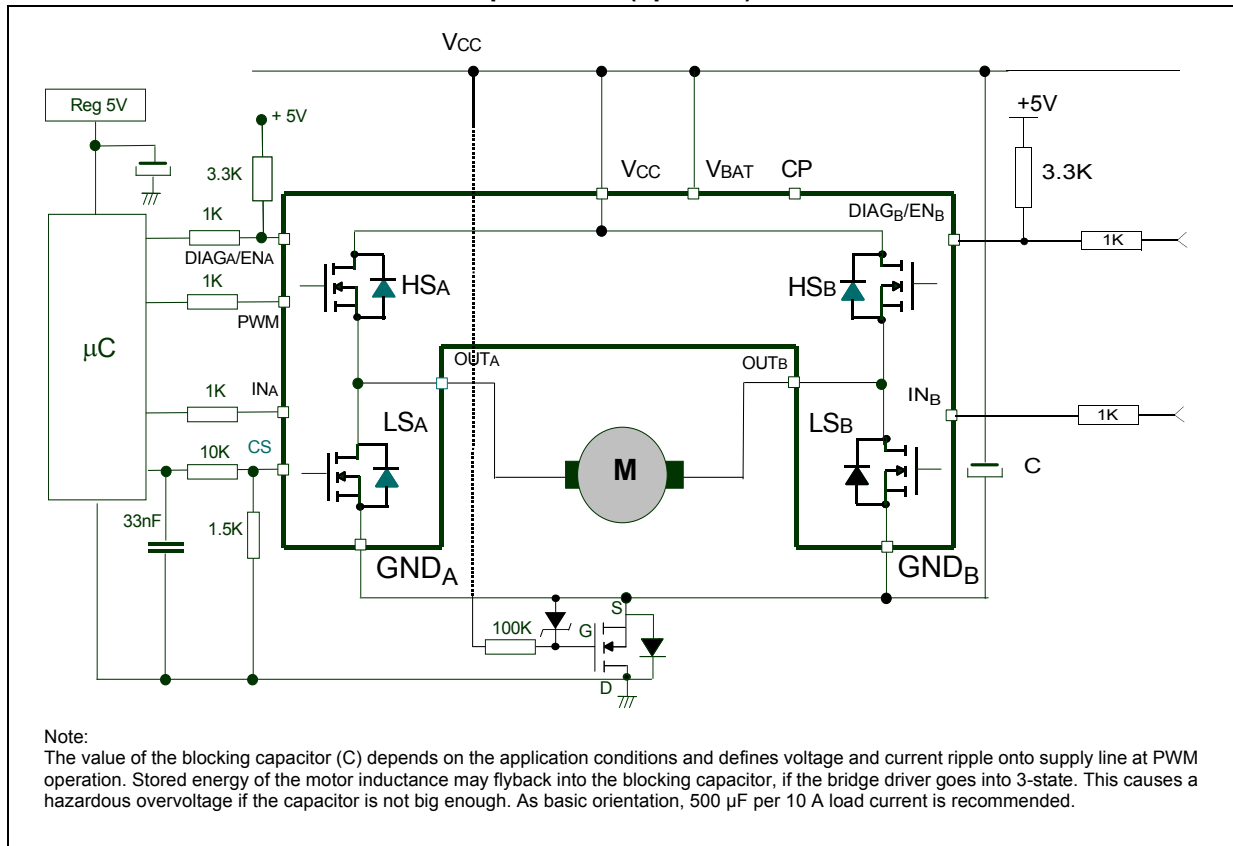


Table 13. Truth table in fault conditions (detected on OUT<sub>A</sub>)

IN <sub>A</sub>	IN <sub>B</sub>	DIAG <sub>A</sub> /EN <sub>A</sub>	DIAG <sub>B</sub> /EN <sub>B</sub>	OUT <sub>A</sub>	OUT <sub>B</sub>	CS (V <sub>CS</sub> =0V)
1	1	0	1	OPEN	H	High impedance
	0				L	
0	1				H	I <sub>OUTB</sub> /K
	0				L	High impedance
X	X		0	OPEN		

↑                      ↑
↑                      ↑  
 Fault Information                      Protection Action

Note: In normal operating conditions the DIAG<sub>X</sub>/EN<sub>X</sub> pin is considered an input pin by the device. This pin must be externally pulled high.

In case of a fault condition the DIAG<sub>X</sub>/EN<sub>X</sub> pin is considered an output pin by the device.



The fault conditions are:

- overtemperature on one or both high-sides (for example, if a short to ground occurs as it could be the case described in line 1 and 2 in the [Table 14](#));
- Short to battery condition on the output (saturation detection on the low-side Power MOSFET).

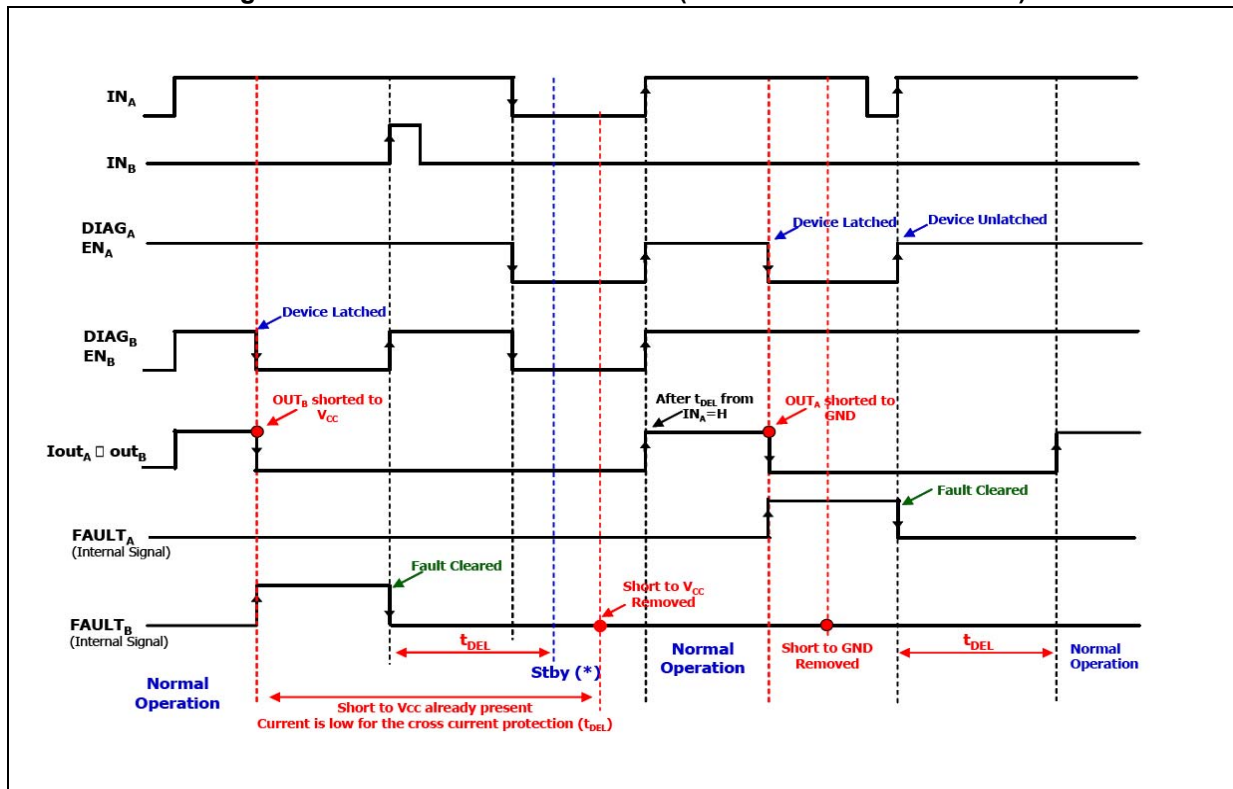
Possible origins of fault conditions may be:

- $OUT_A$  is shorted to ground. It follows that, high-side A is in overtemperature state.
- $OUT_A$  is shorted to  $V_{CC}$ . It follow that, low-side Power MOSFET is in saturation state.

When a fault condition is detected, the user can know which power element is in fault by monitoring the  $IN_A$ ,  $IN_B$ ,  $DIAG_A/EN_A$  and  $DIAG_B/EN_B$  pins.

In any case, when a fault is detected, the faulty leg of the bridge is latched off. To turn-on the respective output ( $OUT_X$ ) again, the input signal must rise from low-level to high-level.

**Figure 6. Behavior in fault condition (how a fault can be cleared)**



Note: In case of the fault condition is not removed, the procedure for unlatching and sending the device in Stby mode is:

- Clear the fault in the device (toggle:  $IN_A$  if  $EN_A=0$  or  $IN_B$  if  $EN_B=0$ )
- Pull low all inputs, PWM and Diag/EN pins within  $t_{DEL}$ .

If the Diag/En pins are already low, PWM=0, the fault can be cleared simply toggling the input. The device enters in stby mode as soon as the fault is cleared.

**Table 14. Electrical transient requirements (part 1)**

ISO T/R 7637/1 Test pulse	Test level				Delay and impedance
	I	II	III	IV	
1	-25 V	-50 V	-75 V	-100 V	2 ms, 10 Ω
2	+25 V	+50 V	+75 V	+100 V	0.2 ms, 10 Ω
3a	-25 V	-50 V	-100 V	-150 V	0.1 μs, 50 Ω
3b	+25 V	+50 V	+75 V	+100 V	0.1 μs, 50 Ω
4	-4 V	-5 V	-6 V	-7 V	100 ms, 0.01 Ω
5	+26.5 V	+46.5 V	+66.5 V	+86.5 V	400 ms, 2 Ω

**Table 15. Electrical transient requirements (part 2)**

ISO T/R 7637/1 Test pulse	Test levels			
	I	II	III	IV
1	C	C	C	C
2	C	C	C	C
3a	C	C	C	C
3b	C	C	C	C
4	C	C	C	C
5	C	E	E	E

**Table 16. Electrical transient requirements (part 3)**

Class	Contents
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device are not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device.

## 2.5 Reverse battery protection

Against reverse battery condition the charge pump feature allows to use an external N-channel MOSFET connected as shown in the typical application circuit (see [Figure 4](#)).

As alternative option, a N-channel MOSFET connected to GND pin can be used (see typical application circuit in figure [Figure 5](#)).

With this configuration we recommend to short V<sub>BAT</sub> pin to V<sub>CC</sub>.

The device sustains no more than -30 A in reverse battery conditions because of the two body diodes of the power MOSFETs. Additionally, in reverse battery condition the I/Os of VNH5019A-E is pulled-down to the V<sub>CC</sub> line (approximately -1.5 V). Series resistor must be inserted to limit the current sunk from the microcontroller I/Os. If I<sub>Rmax</sub> is the maximum target reverse current through microcontroller I/Os, series resistor is:

$$R = \frac{V_{IOs} - V_{CC}}{I_{Rmax}}$$

Figure 7. Definition of the delay time measurement

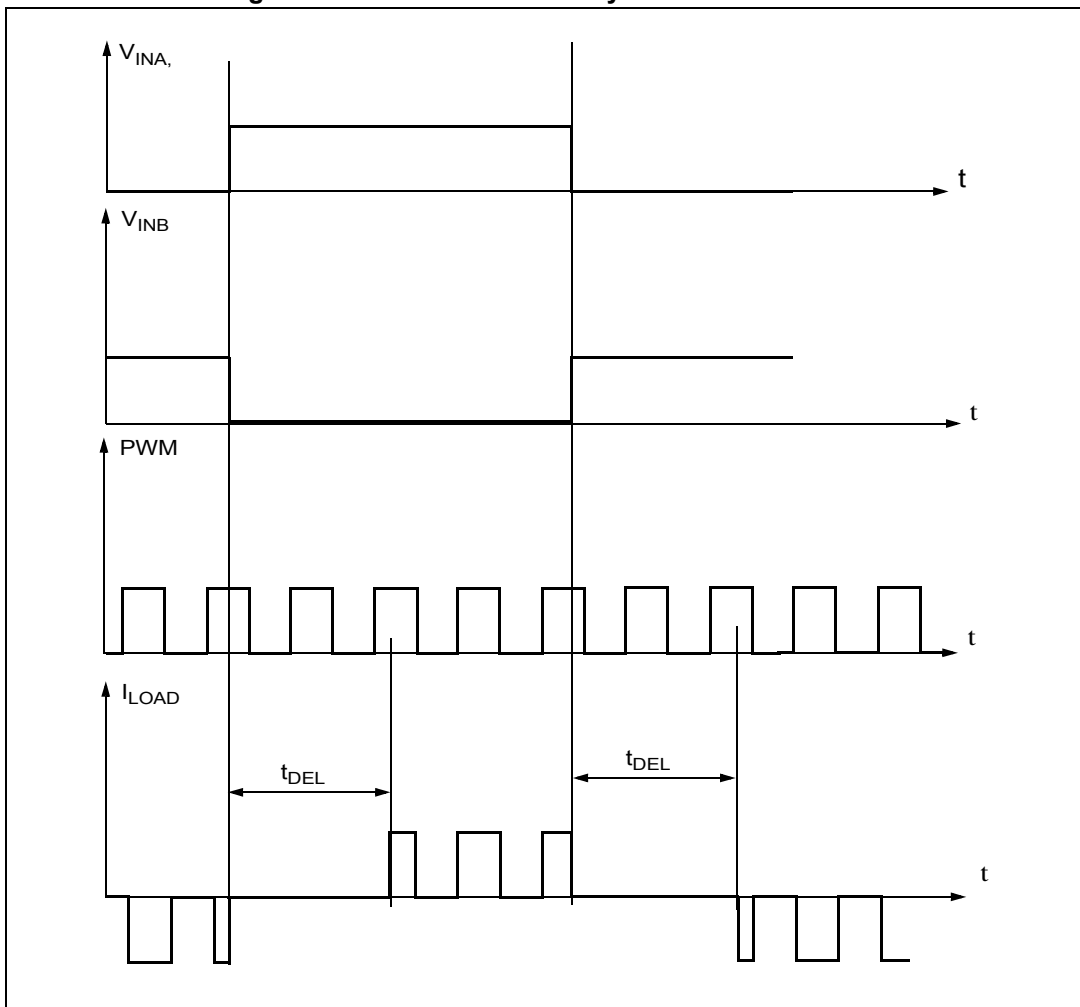


Figure 8. Definition of the low-side switching times

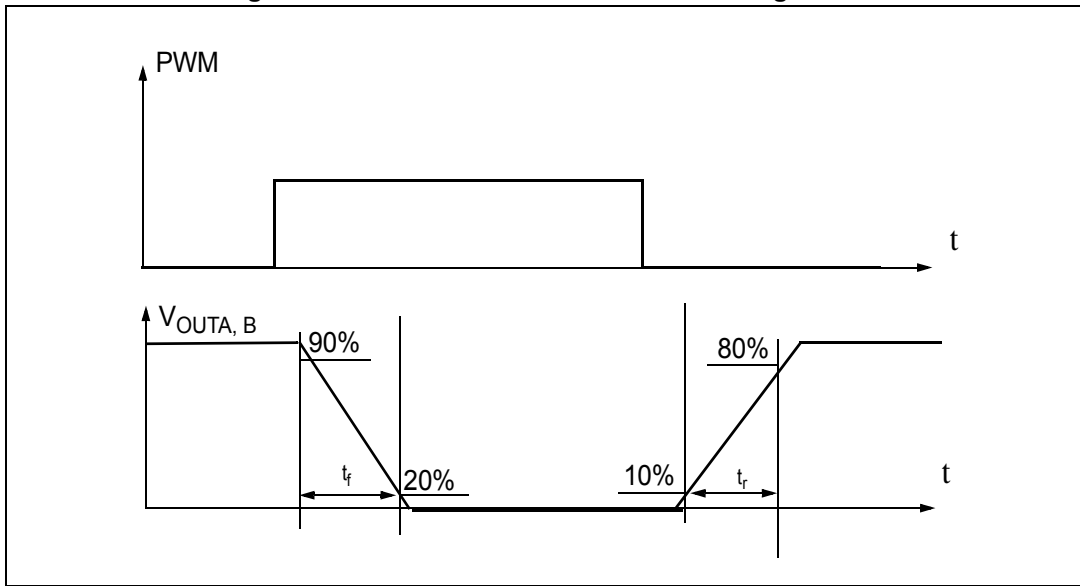


Figure 9. Definition of the high-side switching times

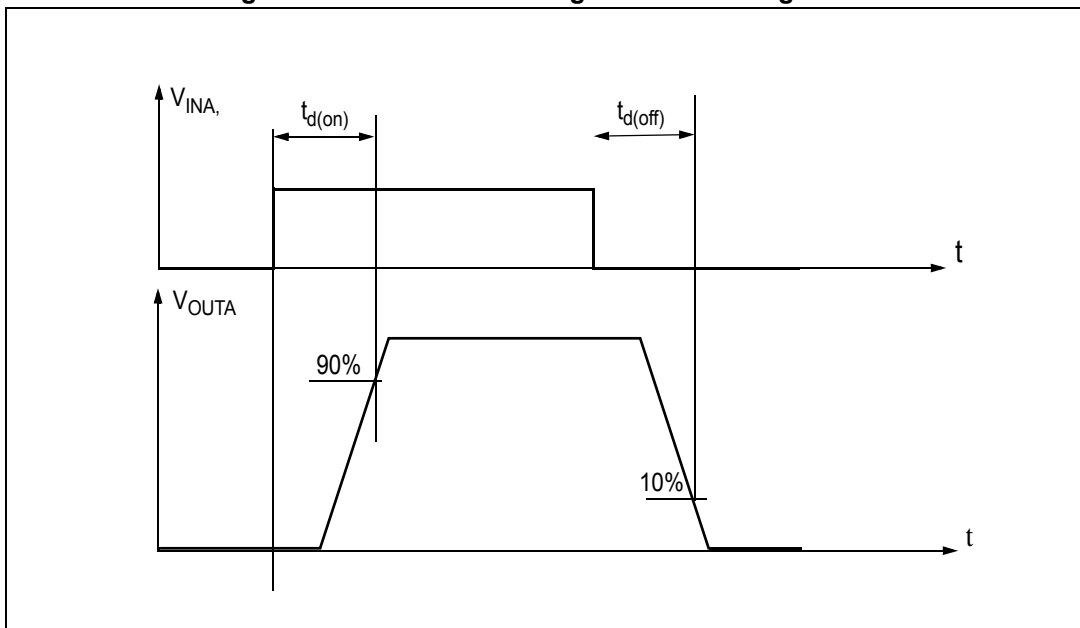


Figure 10. Definition of dynamic cross conduction current during a PWM operation

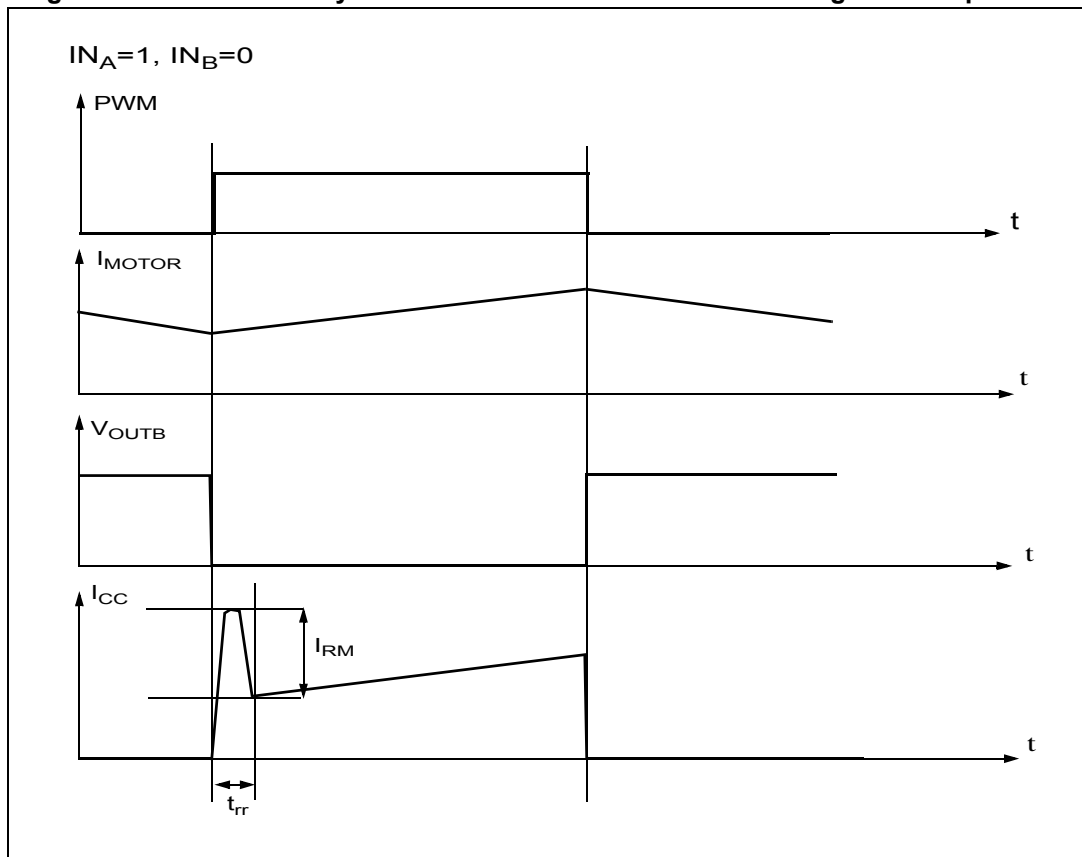


Figure 11. Waveforms in full bridge operation (part 1)

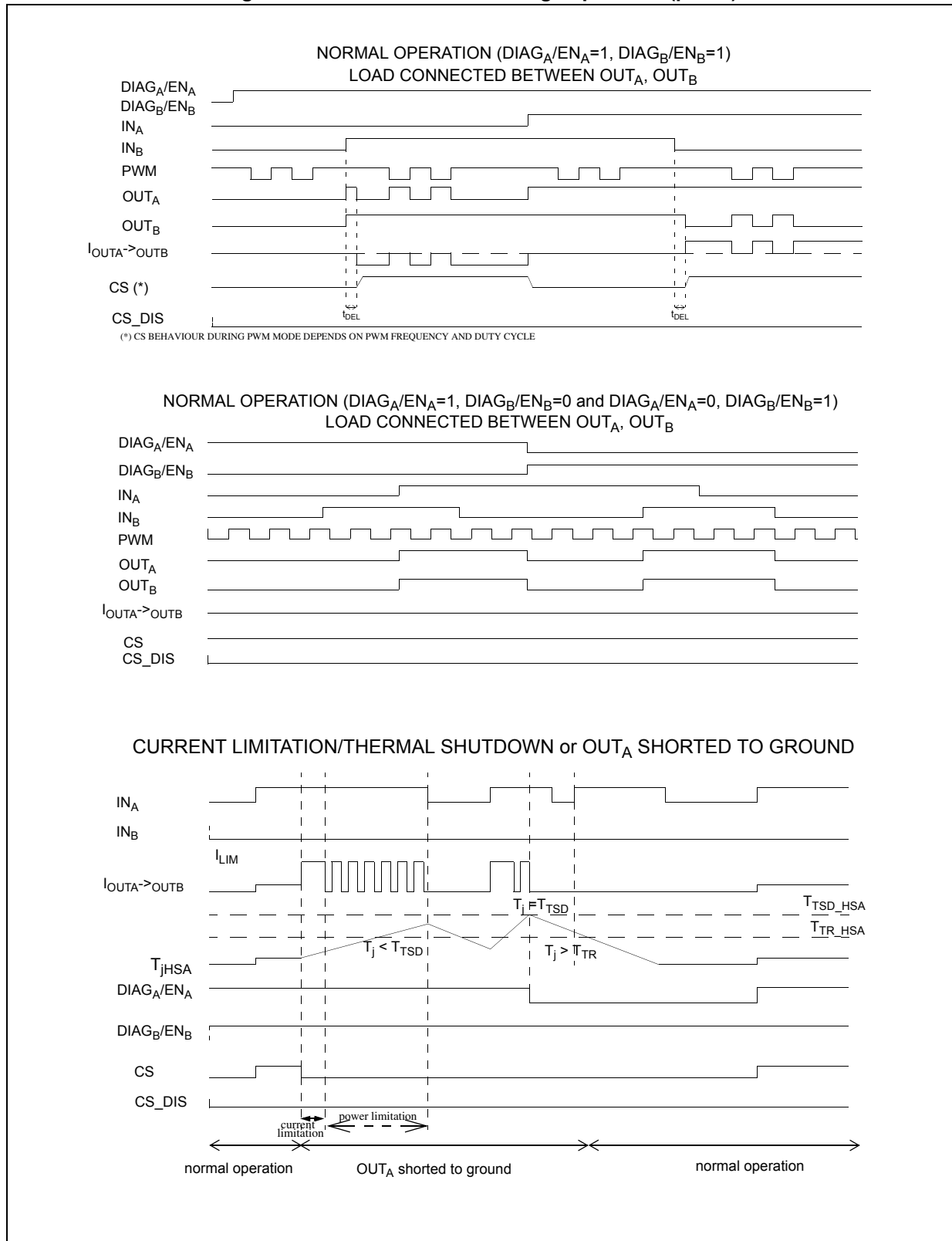
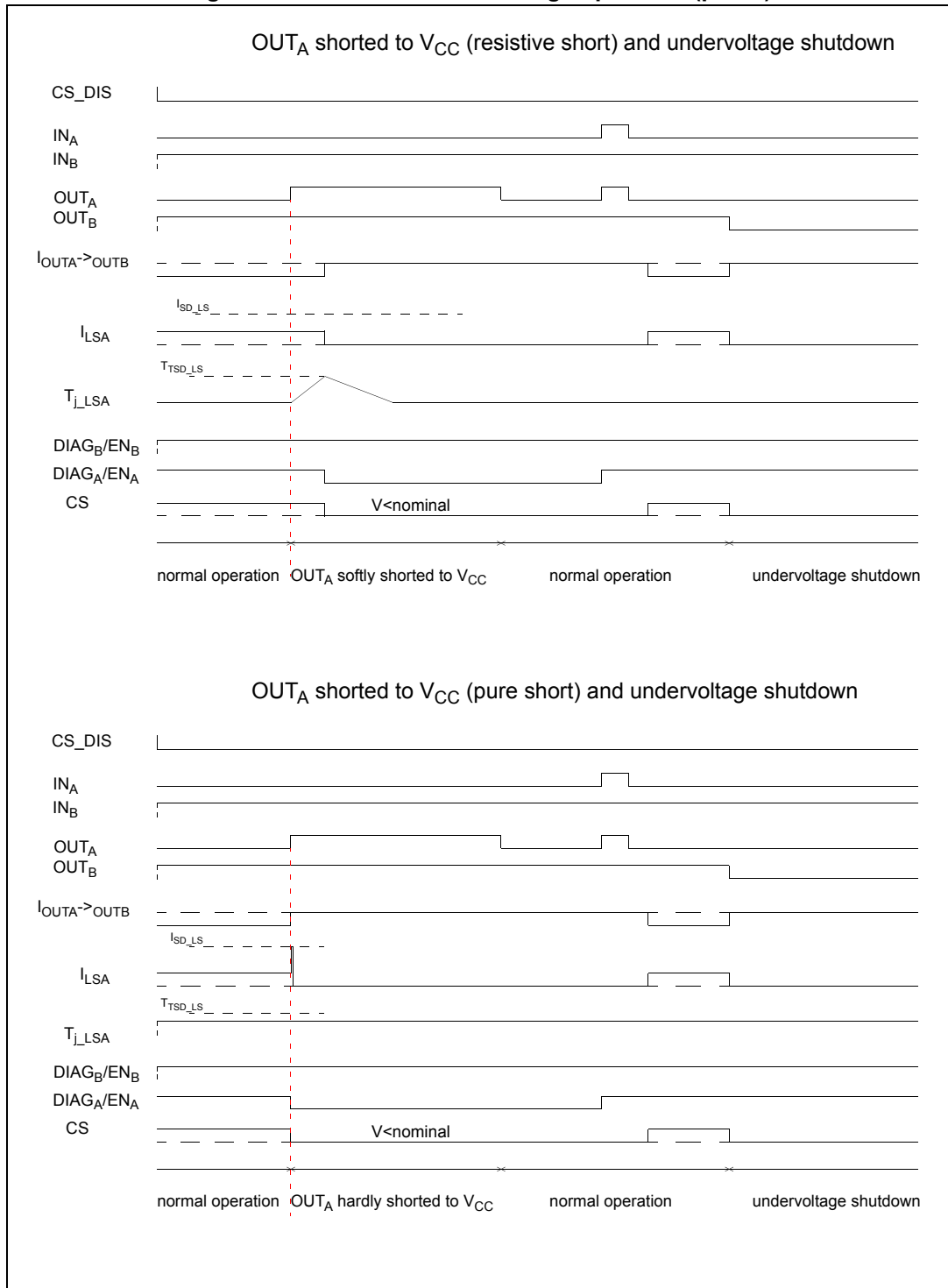
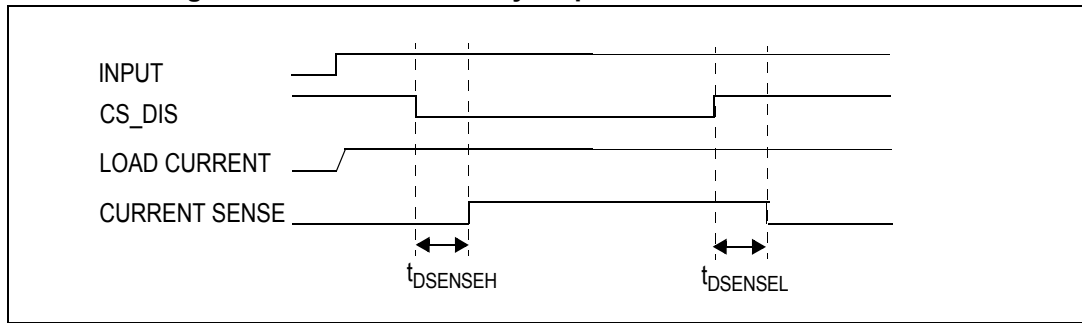


Figure 12. Waveforms in full bridge operation (part 2)

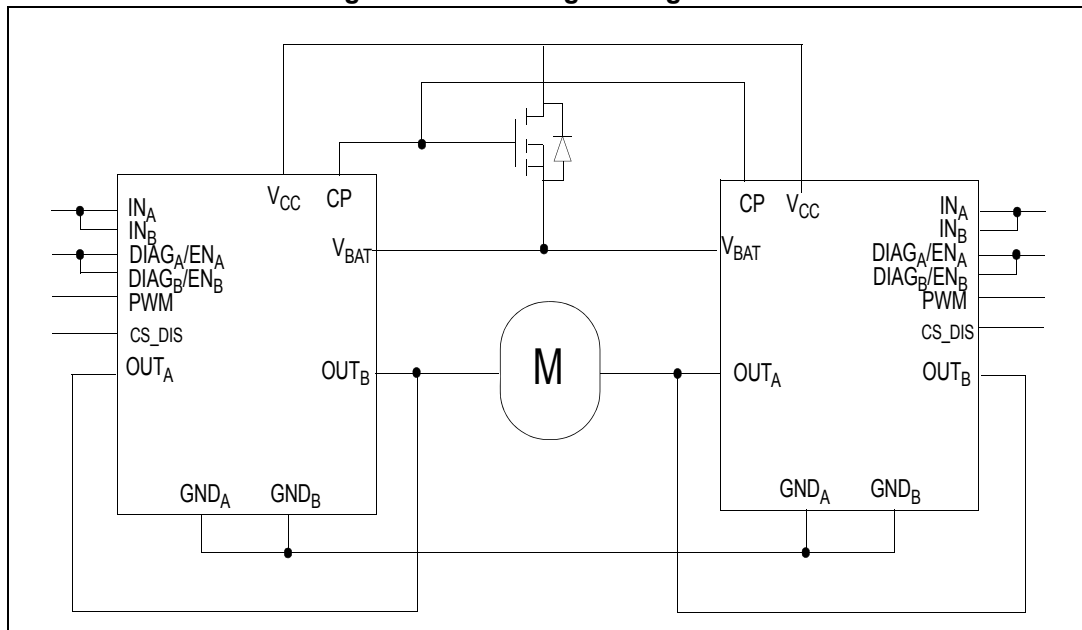


**Figure 13. Definition of delay response time of sense current**



The VNH5019A-E can be used as a high power half-bridge driver achieving an on-resistance per leg of 9.5 mΩ. The figure below shows the suggested configuration:

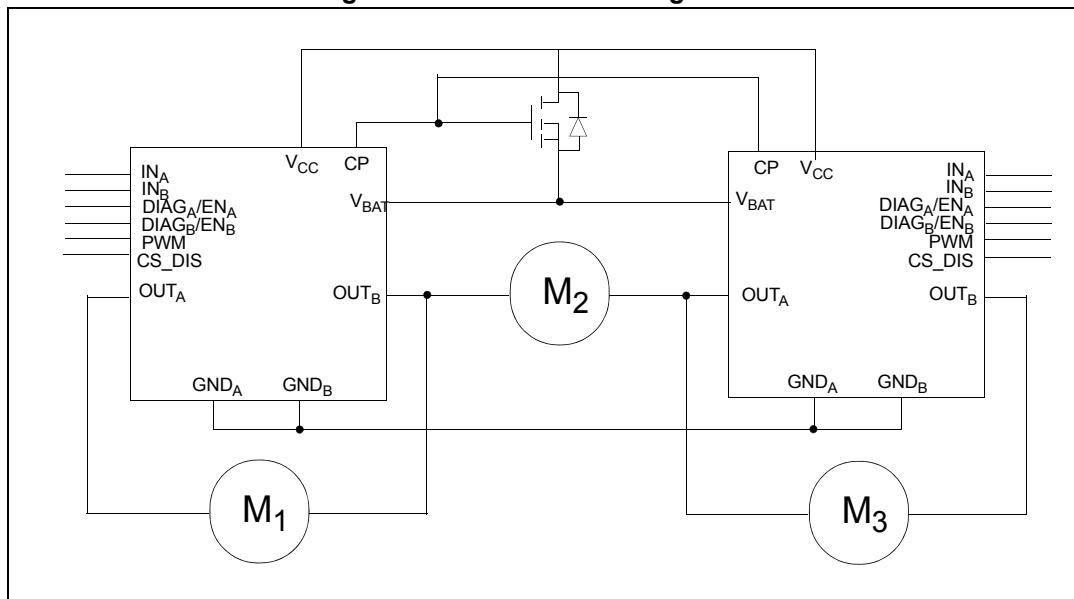
**Figure 14. Half-bridge configuration**



The VNH5019A-E can easily be designed in multi-motor driving applications such as seat positioning systems where only one motor must be driven at a time. The DIAG<sub>x</sub>/EN<sub>x</sub> pins allow the unused half-bridges to be put into high-impedance. The diagram that follows shows the suggested configuration:



Figure 15. Multi-motor configuration



### 3 Package and PCB thermal data

#### 3.1 MultiPowerSO-30 thermal data

Figure 16. MultiPowerSO-30™ PC board

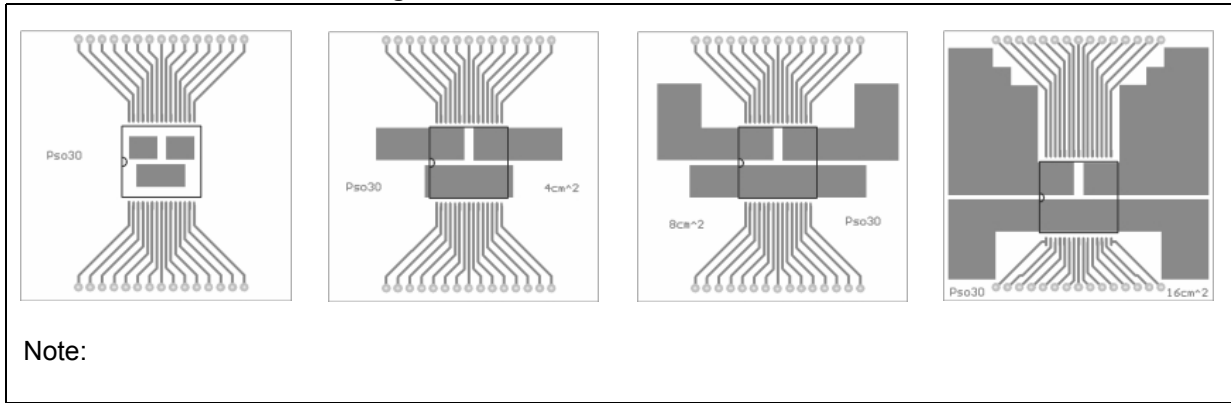


Figure 17. Chipset configuration

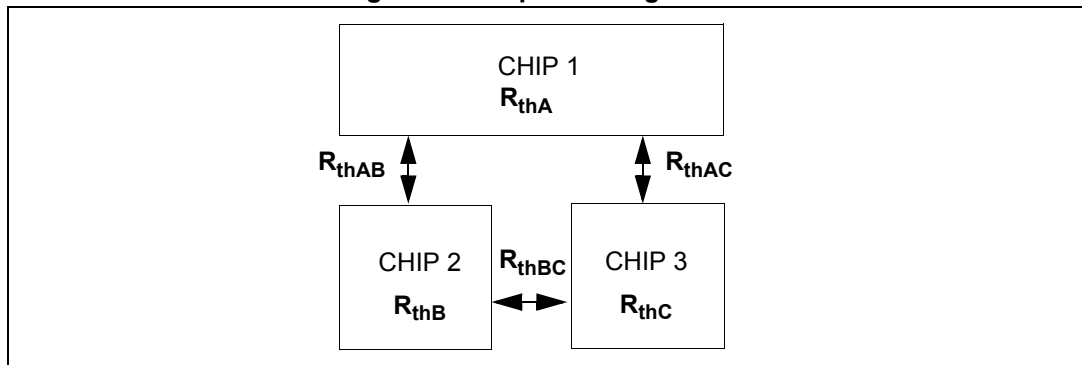
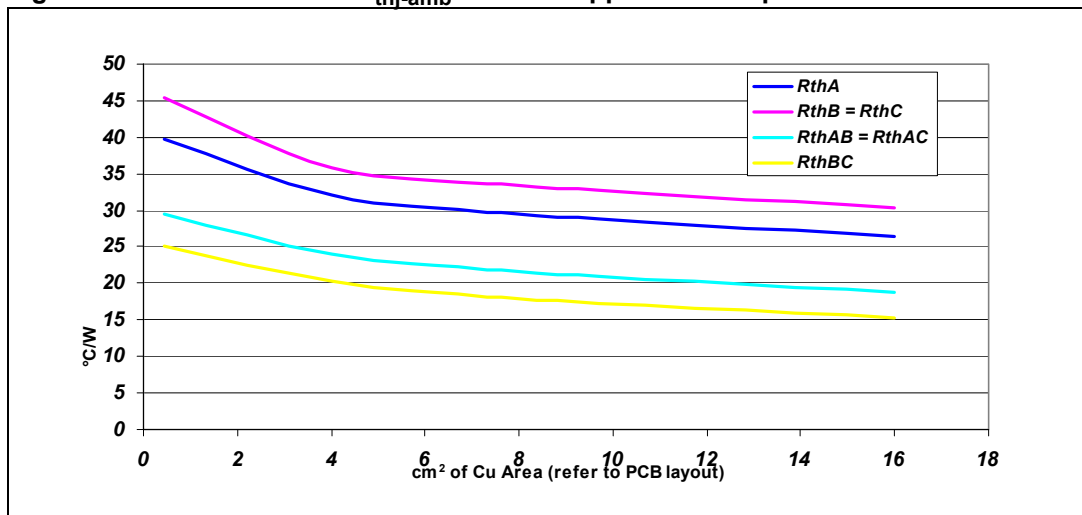


Figure 18. Auto and mutual  $R_{thj-amb}$  vs PCB copper area in open box free air condition



### 3.1.1 Thermal calculation in clockwise and anti-clockwise operation in steady-state mode

Table 17. Thermal calculation in clockwise and anti-clockwise operation in steady-state mode

Chip 1	Chip 2	Chip 3	Tjchip1	Tjchip2	Tjchip3
ON	OFF	ON	$\frac{P_{dchip1} \cdot R_{thA} + P_{dchip3} \cdot R_{thAC} + T_{amb}}{R_{thAC} + T_{amb}}$	$\frac{P_{dchip1} \cdot R_{thAB} + P_{dchip3} \cdot R_{thBC} + T_{amb}}{R_{thBC} + T_{amb}}$	$\frac{P_{dchip1} \cdot R_{thAC} + P_{dchip3} \cdot R_{thC} + T_{amb}}{R_{thC} + T_{amb}}$
ON	ON	OFF	$\frac{P_{dchip1} \cdot R_{thA} + P_{dchip2} \cdot R_{thAB} + T_{amb}}{R_{thAB} + T_{amb}}$	$\frac{P_{dchip1} \cdot R_{thAB} + P_{dchip2} \cdot R_{thB} + T_{amb}}{R_{thAB} + T_{amb}}$	$\frac{P_{dchip1} \cdot R_{thAC} + P_{dchip2} \cdot R_{thBC} + T_{amb}}{R_{thBC} + T_{amb}}$
ON	OFF	OFF	$P_{dchip1} \cdot R_{thA} + T_{amb}$	$P_{dchip1} \cdot R_{thAB} + T_{amb}$	$P_{dchip1} \cdot R_{thAC} + T_{amb}$
ON	ON	ON	$\frac{P_{dchip1} \cdot R_{thA} + (P_{dchip2} + P_{dchip3}) \cdot R_{thAB} + T_{amb}}{R_{thAB} + T_{amb}}$	$\frac{P_{dchip2} \cdot R_{thB} + P_{dchip1} \cdot R_{thAB} + P_{dchip3} \cdot R_{thBC} + T_{amb}}{R_{thAB} + P_{dchip3} \cdot R_{thBC} + T_{amb}}$	$\frac{P_{dchip1} \cdot R_{thAB} + P_{dchip2} \cdot R_{thBC} + P_{dchip3} \cdot R_{thC} + T_{amb}}{R_{thBC} + P_{dchip3} \cdot R_{thC} + T_{amb}}$

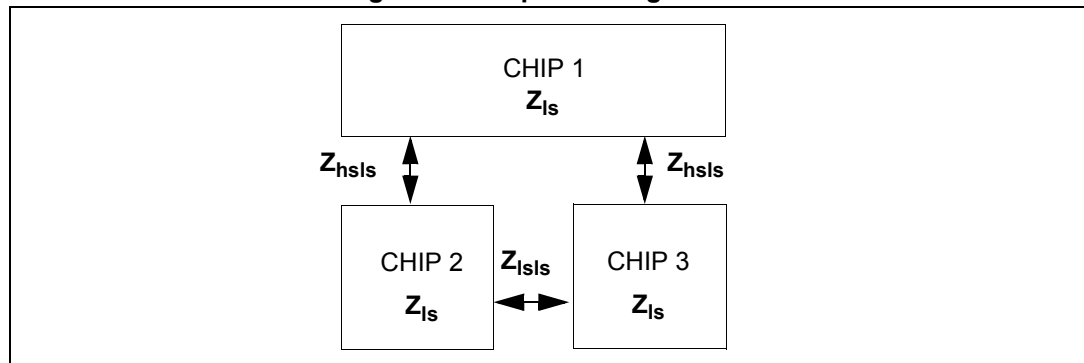
### 3.1.2 Thermal calculation in transient mode

$$T_{hs} = P_{dhs} \cdot Z_{hs} + Z_{hsls} \cdot (P_{dIsA} + P_{dIsB}) + T_{amb}$$

$$T_{IsA} = P_{dIsA} \cdot Z_{Is} + P_{dhs} \cdot Z_{hsls} + P_{dIsB} \cdot Z_{hsls} + T_{amb}$$

$$T_{IsB} = P_{dIsB} \cdot Z_{Is} + P_{dhs} \cdot Z_{hsls} + P_{dIsA} \cdot Z_{hsls} + T_{amb}$$

Figure 19. Chipset configuration



Equation 1: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where  $\delta = t_p/T$

Figure 20. MultiPowerSO-30 HSD thermal impedance junction ambient single pulse

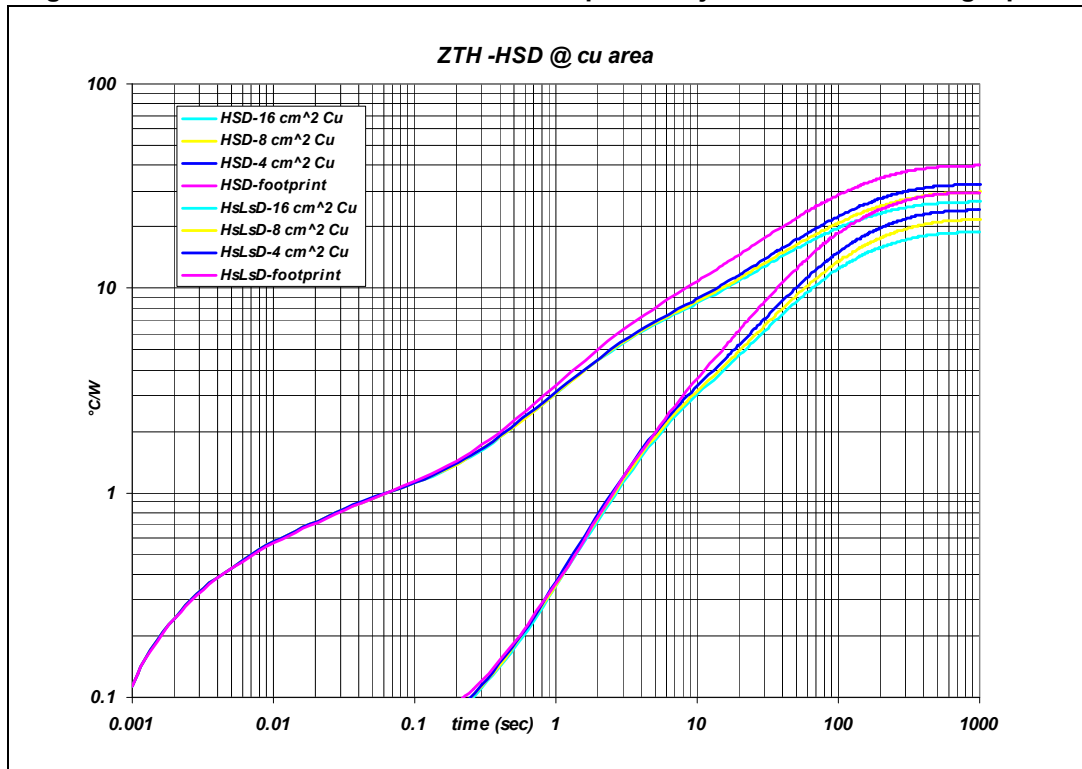


Figure 21. MultiPowerSO-30 LSD thermal impedance junction ambient single pulse

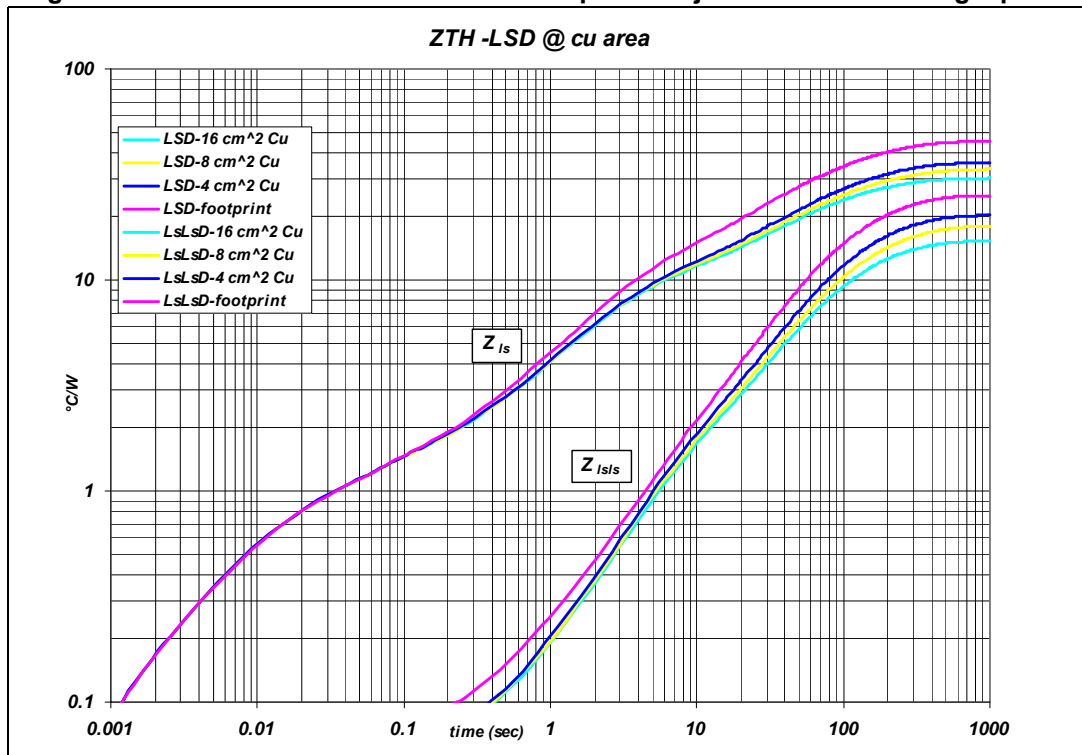


Figure 22. Thermal fitting model of an H-bridge in MultiPowerSO-30

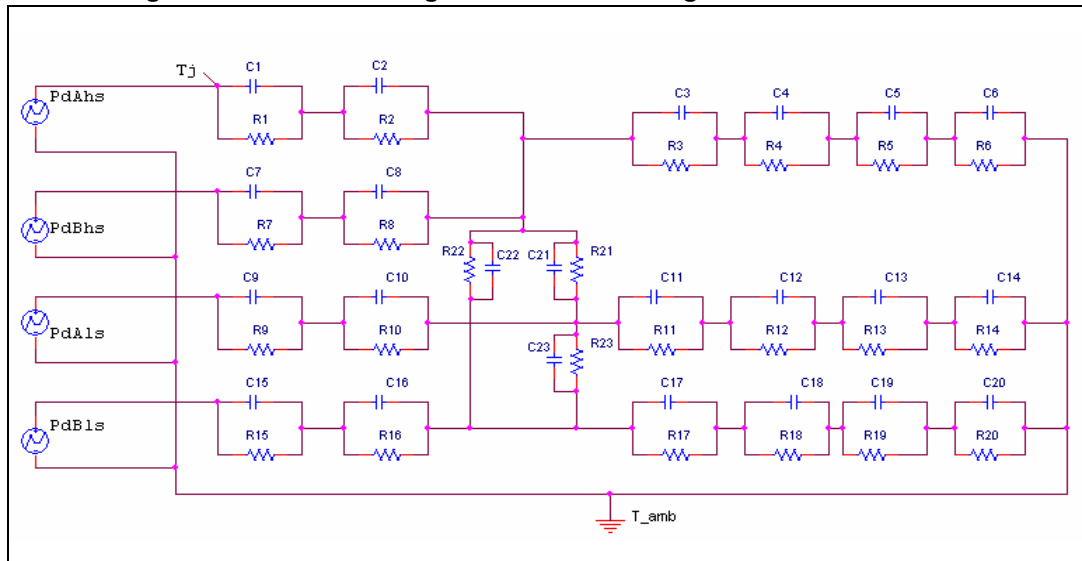


Table 18. Thermal parameters<sup>(1)</sup>

Area/island (cm <sup>2</sup> )	Footprint	4	8	16
R1 = R7 (°C/W)	0.1			
R2 = R8 (°C/W)	0.3			
R3 = R10 = R16 (°C/W)	0.5			
R4 (°C/W)	6			
R5 (°C/W)	30	24	24	24
R6 (°C/W)	56	52	42	32
R9 = R15 (°C/W)	0.05			
R11 = R17 (°C/W)	0.7			
R12 = R18 (°C/W)	10			
R13 = R19 (°C/W)	36	26	26	26
R14 = R20 (°C/W)	56	42	36	28
R21 = R22 (°C/W)	35	25	25	25
R23 (°C/W)	160	150	150	150
C1 = C7 = C9 = C15 (W.s/°C)	0.005			
C2 = C8 (W.s/°C)	0.01			
C3 (W.s/°C)	0.03			
C4 (W.s/°C)	0.4			
C5 (W.s/°C)	1.5	2	2	2
C6 (W.s/°C)	3	4	5	6
C10 = C16 (W.s/°C)	0.015			
C11 = C17 (W.s/°C)	0.05			

Table 18. Thermal parameters<sup>(1)</sup> (continued)

Area/island (cm <sup>2</sup> )	Footprint	4	8	16
C12 = C18 (W.s/°C)	0.3			
C13 = C19 (W.s/°C)	1.2	2	2	2
C14 = C20 (W.s/°C)	2.5	3	4	5
C21 = C22 = C23 (W.s/°C)	0.01	0.008	0.008	0.008

1. A blank space means that the value is the same as the previous one.

## 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

### 4.1 MultiPowerSO-30 package information

Figure 23. MultiPowerSO-30 package outline

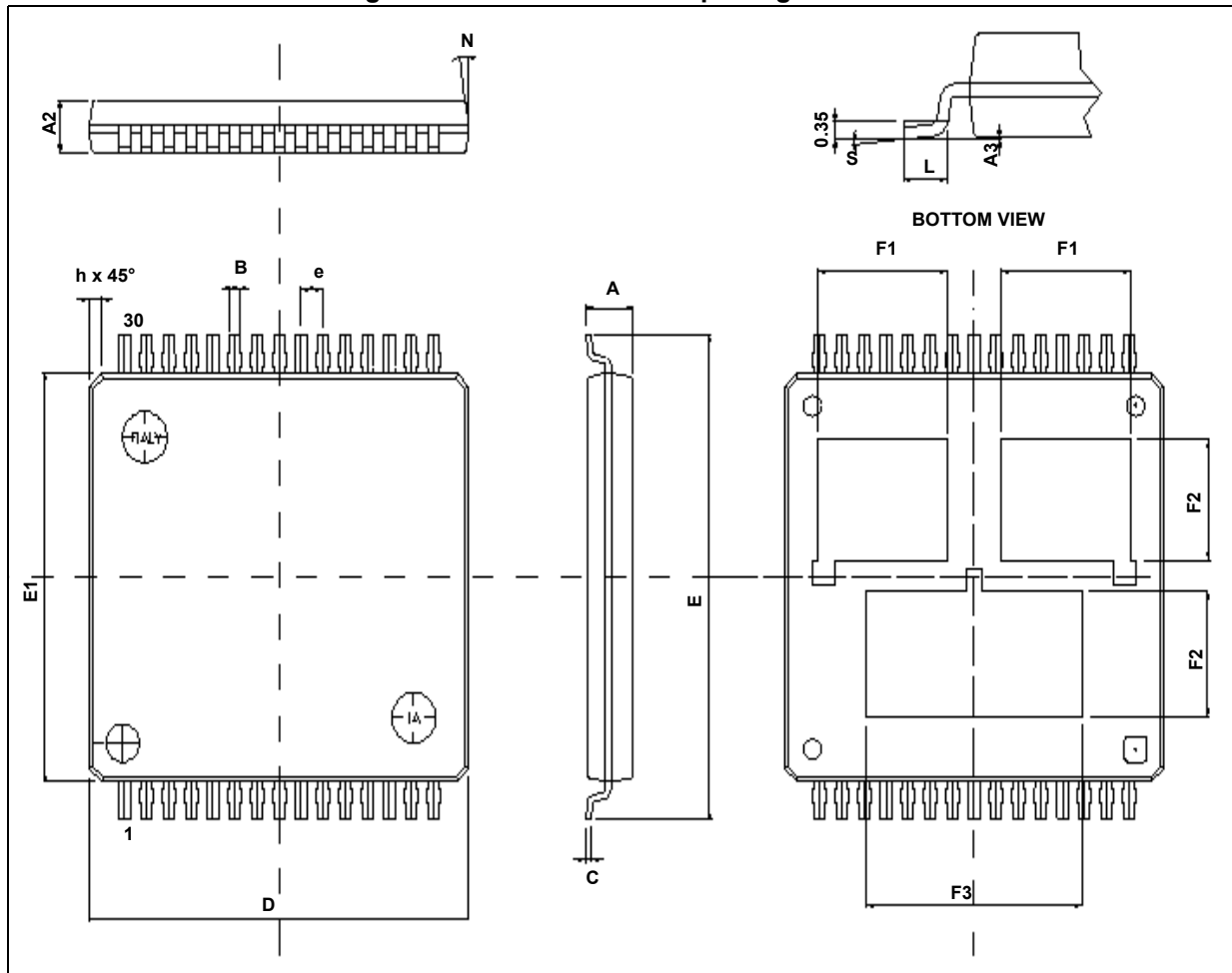


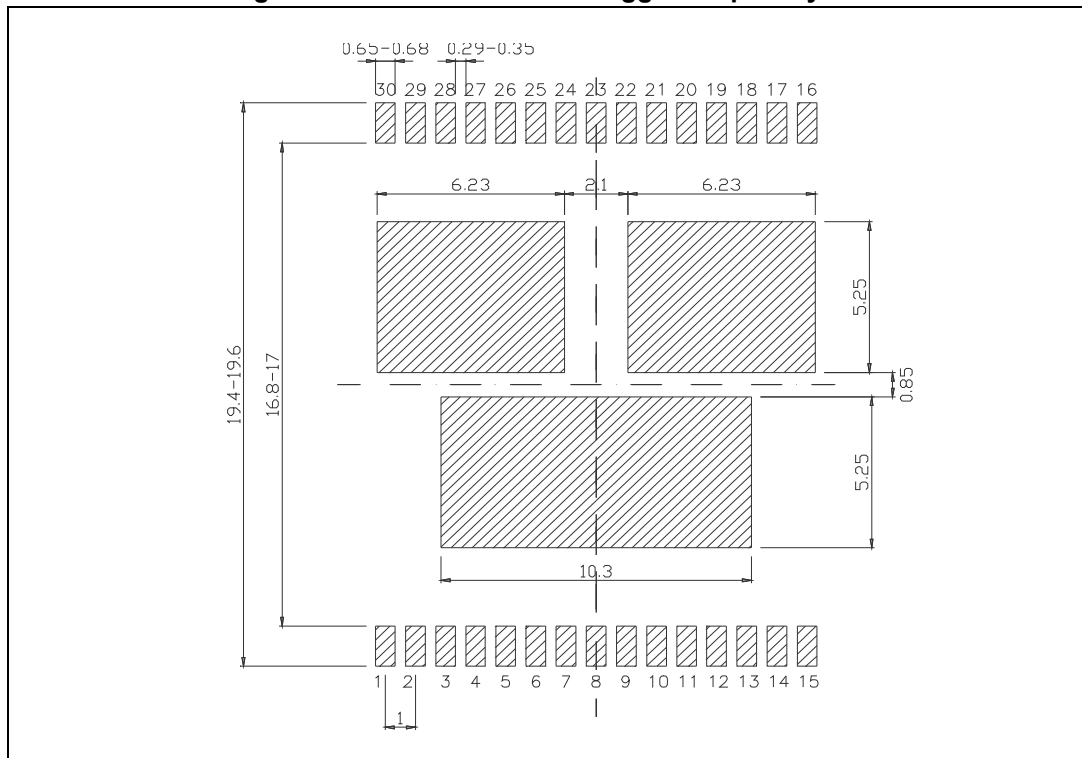
Table 19. MultiPowerSO-30 mechanical data

Symbol	Data book mm		
	Min.	Typ.	Max.
A			2.35
A2	1.85		2.25
A3	0		0.1
B	0.42		0.58
C	0.23		0.32
D	17.1	17.2	17.3
E	18.85		19.15
E1	15.9	16	16.1
e		1	
F1	5.55		6.05
F2	4.6		5.1
F3	9.6		10.1
L	0.8		1.15
N			10°
S	0°		7°



## 4.2 MultiPowerSO-30 suggested land pattern

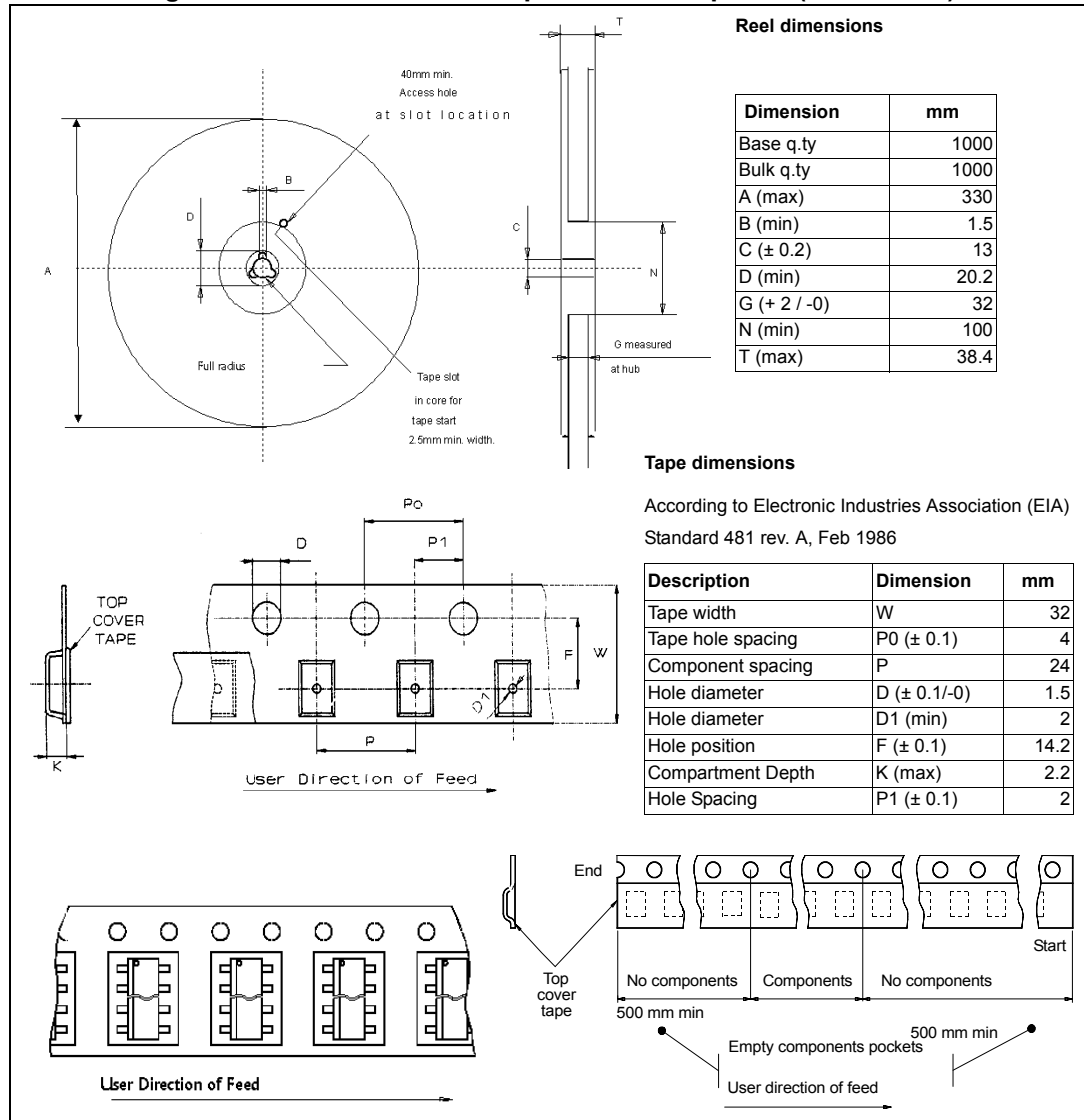
Figure 24. MultiPowerSO-30 suggested pad layout



### 4.3 MultiPowerSO-30 packing information

The devices are packed in tape and reel shipments (see [Figure 20: Device summary on page 35](#)).

**Figure 25. MultiPowerSO-30 tape and reel shipment (suffix “TR”)**



## 5 Order codes

Table 20. Device summary

Package	Order codes
	Tape and reel
MultiPowerSO-30	VNH5019TR-E

## 6 Revision history

**Table 21. Document revision history**

Date	Revision	Changes
22-Jan-2008	1	Initial release.
04-Nov-2009	2	<p>Uploaded corporate template by using V3 version</p> <p>Added <i>Table 5: Thermal data</i></p> <p><i>Section 2.1: Absolute maximum ratings</i></p> <ul style="list-style-type: none"> <li>– Added text</li> </ul> <p><i>Table 6: Power section</i></p> <ul style="list-style-type: none"> <li>– <math>I_S</math>: added max value for <math>I_{N_A} = I_{N_B} = PWM = 0</math>; <math>T_j = 25\text{ }^\circ\text{C}</math>; <math>V_{CC}=13\text{V}</math> in Test conditions, deleted <math>I_{N_A} = I_{N_B} = PWM = 0</math></li> <li>– <math>V_f</math>: changed Test conditions, changed typ/max value</li> <li>– <math>I_{RM}</math>: deleted and copied in <i>Table 8: Switching (<math>V_{CC} = 13\text{ V}</math>, <math>R_{LOAD} = 0.87\text{ W}</math>, <math>T_j = 25\text{ }^\circ\text{C}</math>)</i> whole row</li> </ul> <p><i>Table 8: Switching (<math>V_{CC} = 13\text{ V}</math>, <math>R_{LOAD} = 0.87\text{ W}</math>, <math>T_j = 25\text{ }^\circ\text{C}</math>)</i></p> <ul style="list-style-type: none"> <li>– <math>t_{DEL}</math>: changed min/typ/max value</li> <li>– Copied <math>I_{RM}</math> row by <i>Table 6: Power section</i></li> </ul> <p>Updated <i>Table 10: Current sense (<math>8\text{ V} &lt; V_{CC} &lt; 21\text{ V}</math>)</i></p> <p><i>Table 11: Charge pump</i></p> <ul style="list-style-type: none"> <li>– <math>V_{CP}</math>: changed min/max value for <math>EN_X = 5\text{ V}</math>, changed typ value for <math>EN_X = 5\text{ V}</math>, <math>V_{CC} = 4.5\text{ V}</math></li> </ul> <p>Updated <i>Figure 11: Waveforms in full bridge operation (part 1)</i></p> <p>Updated <i>Figure 12: Waveforms in full bridge operation (part 2)</i></p> <p>Added <i>Chapter 4</i></p>
16-Dec-2009	3	<p>Updated following tables:</p> <ul style="list-style-type: none"> <li>– <i>Table 6: Power section</i></li> <li>– <i>Table 9: Protection and diagnostic</i></li> <li>– <i>Table 10: Current sense (<math>8\text{ V} &lt; V_{CC} &lt; 21\text{ V}</math>)</i></li> </ul> <p>Added <i>Figure 6: Behavior in fault condition (how a fault can be cleared)</i></p> <p>Added <i>Chapter 3: Package and PCB thermal data</i></p>
06-Apr-2010	4	<p>Updated <i>Table 5: Thermal data</i>.</p> <p><i>Table 6: Power section:</i></p> <ul style="list-style-type: none"> <li>– <math>I_S</math>: updated test condition and max value</li> </ul> <p>Updated table notes on <i>Table 9: Protection and diagnostic</i>.</p> <p><i>Table 10: Current sense (<math>8\text{ V} &lt; V_{CC} &lt; 21\text{ V}</math>):</i></p> <ul style="list-style-type: none"> <li>– <math>dK_0/k_0</math>, <math>dK_1/k_1</math>, <math>dK_3/k_3</math>: updated minimum end maximum values.</li> </ul>
19-Apr-2010	5	Updated <i>Table 10: Current sense (<math>8\text{ V} &lt; V_{CC} &lt; 21\text{ V}</math>)</i> .
25-May-2010	6	<p>Updated <i>Features</i> list.</p> <p>Updated <i>Table 6: Power section</i>.</p>
02-Sep-2010	7	Updated <i>Table 5: Thermal data</i> .

Table 21. Document revision history (continued)

Date	Revision	Changes
22-Dec-2011	8	Updated <i>Figure 1: Block diagram</i> Added <i>Table 1: Suggested connections for unused and not connected pins</i> Updated <i>Table 3: Block descriptions</i> <i>Table 8: Switching (<math>V_{CC} = 13\text{ V}</math>, <math>R_{LOAD} = 0.87\text{ W}</math>, <math>T_j = 25\text{ °C}</math>):</i> – $T_{TSD}$ , $T_{TR}$ , $T_{HYST}$ : added note – $T_{TSD\_LS}$ : added row Updated <i>Table 13: Truth table in fault conditions (detected on OUTA)</i> Updated <i>Figure 11: Waveforms in full bridge operation (part 1)</i> and <i>Figure 12: Waveforms in full bridge operation (part 2)</i>
19-Sep-2013	9	Updated Disclaimer.
11-Jan-2017	10	– Removed all information relative to tube packing of the product – Modified <a href="#">Section 4: Package information</a> . – Added AEC-Q100 qualified in the Features section – Minor text edits throughout the document

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